# A NEW MEMRISTOR IMPLEMENTATION AND ITS APPLICATIONS IN ANALOG CIRCUITS

BY

**Zainulabideen Jamal Khalifa**

A Thesis Presented to the

DEANSHIP OF GRADUATE STUDIES

**KING FAHD UNIVERSITY OF PETROLEUM & MINERALS**

DHAHRAN, SAUDI ARABIA

In Partial Fulfillment of the
Requirements for the Degree of

# MASTER OF SCIENCE

**In**

**Electrical Engineering**

**May, 2014**

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

DHAHRAN- 31261, SAUDI ARABIA

**DEANSHIP OF GRADUATE STUDIES**

This thesis, written by **Zainulabideen Jamal Khalifa** under the direction his thesis advisor and approved by his thesis committee, has been presented and accepted by the Dean of Graduate Studies, in partial fulfillment of the requirements for the degree of **MASTER OF SCIENCE IN ELECTRICAL ENGINEERING.**

Dr. Muhammad Taher Abuelma'atti
(Advisor)

Dr. Ali Ahmad Al-Shaikhi
Department Chairman

Dr. Munir A. Kulaib Al-Absi
(Member)

Dr. Salam A. Zummo
Dean of Graduate Studies

Dr. Alaa El-Din Hussein
(Member)

21/5/14
*Date*

# ACKNOWLEDGMENTS

Praise be to ALLAH for giving me the strength and perseverance to complete this thesis. Also, praise be to HIM for blessing me to work with Dr. Muhammad Abuelma'atti and to have a great chance to learn from him and to be my advisor in this thesis.

I would like to acknowledge the effort and patience of Dr. Muhammad Abuelma'atti and I thank him for that. Also, special thanks to Dr. Munir and Dr. Alaa for their support and for accepting to be in my committee.

Special thanks to my mother who pushed me and supported me all the way to reach where I am now. She was a great contributor to motivate me and support me. Also, I must acknowledge my wife's support and the sacrifices she made for me to finish this thesis. I would like to thank my friends who helped me in discussions and who helped to widen my view on the subject, Mr. Eyas and Mr. Nayef.

# TABLE OF CONTENTS

# LIST OF FIGURES

# LIST OF TABLES

# ABSTRACT

Full Name : Zainulabideen Jamal Khalifa

Thesis Title : A New Memristor Implementation and Its Applications in Analog Circuits

Major Field : Electrical Engineering

Date of Degree : May, 2014

This thesis studies various memristor emulators and surveys different memristor-based analog applications. Different circuit emulators have been proposed to suit different conditions in analog circuits. These emulator types include voltage or current driven emulator, floating or grounded emulator, discrete or continuous memristance level emulator, multi-state levels emulator, incremental or decremental emulator and finally a negative memristor emulator. Some memristor-based applications have been implemented and tested. Applications in digital modulation such as amplitude shift keying, frequency shift keying and binary phase shift keying are considered. Other applications include sinusoidal oscillator, multivibrating oscillator and chaotic oscillator.

# ملخص الرسالة

**الاسم الكامل**: زين العابدين جمال احمد خليفه

**عنوان الرسالة:** تطبيق جديد للممرستور و استعمالاته في الدوائر التماثلية

**التخصص:** الهندسة الكهربائية

**تاريخ الدرجة العلمية**: مايو2014

تدرس هذه الأطروحة دوائر مختلفة لمحاكاة الممرستور و تتطرق لعدد من التطبيقات التماثلية القائمة على الممرستور. تم اقتراح عدد من دوائر المحاكاة المختلفة لتتناسب مع الظروف المختلفة في الدوائر التماثلية. تشمل هذه الأنواع محاكي ذو الدخل المتأثر بالجهد أو بالتيار أو أن يكون المحاكي عائم أو متصل بالأرضي أو أن يكون ذو مستويات معدودة أو متصلة أو أن يكون ثنائي المستوى أو أن يكون محاكي تراكمي أو تناقصي وأخيرا أن يكون محاكي سلبي القيمة. وقد تم تنفيذ بعض التطبيقات القائمة على الممرستور واختبارها. و منها تطبيقات في التضمين التماثلي مثل تشكيل الموجة على السعة أو تشكيل الموجة على التردد أو التشكيل ثنائي إزاحة الطور. وتشمل التطبيقات الأخرى مذبذب الجيبية و مذبذب الإهتزاز والمذبذب الفوضوي.

# Chapter 1

# Introduction

## 1.1. Motivation

Since its inception by Chua in 1970's, the memristor was just a theoretical element filling a natural pattern gap. It has been so until in 2008 a group from HP labs was able to realize it. Since then, a race has begun among researchers to come up with applications utilizing this element to improve the performance of current applications. Many proposals and attempts are being done using the memristor in digital circuits. Memristor-based digital applications are mainly focusing on improving the performance of memories and in realizing synapses in neural networks. There are also attempts to use the memristor in analog signal processing. Since the memristor is not commercially available as standing alone device, most of these applications are based on a memristor emulator; that is a circuit built using commercially available integrated circuits. Currently used memristor emulators will be studied and new emulators will be introduced in order to improve the performance and shortcomings of the current emulators. For that, the physical characteristics and fingerprints of the memristor must be studied. Analog memristor applications will be surveyed and investigated and some of these applications will be implemented using the proposed circuit emulator of the memristor.

By replacing the resistors with memristors, the memristor offers new possibilities to improve the current circuitries in terms of the size on chips. Moreover, the memristor can provide a variety of new applications. However, the variation in its value must be

taken into considerations not to affect the application. The variation itself is useful and can be used to replace capacitors. This will be shown in the multivibrating oscillator application. The use of such advantage can be very beneficial when a very low frequency is needed such as in medical applications to avoid the use of large values of capacitors as well as resistors. Also, it can give different possibilities of using the memristor in very high frequency applications as well. The non-linearity of the memristor is also useful in chaotic oscillators and can give more variations to what is already there in the literature.

## 1.2. What is the Memristor?

The memristor is considered as a basic two-terminal electrical component that directly relates the charge flow with the flux linkage. This relationship characterize the memristor and it is denoted (M) that is the memristance as defined by equation (2.1). The memristor can be considered as a resistor changing with the flow of charges through it. This change does not revert when the power supply applied is removed giving the memristor the memory property [1]. As more charge flow through its terminals, its state will change to another value of resistance bounded by the limits $R_{ON}$-$R_{OFF}$. A reverse flow of charges revert the state to the previous one. This relates the memristance with the time variable as well. The four basic elements in electrical circuits are shown in relation with each other in Figure 1 [1].

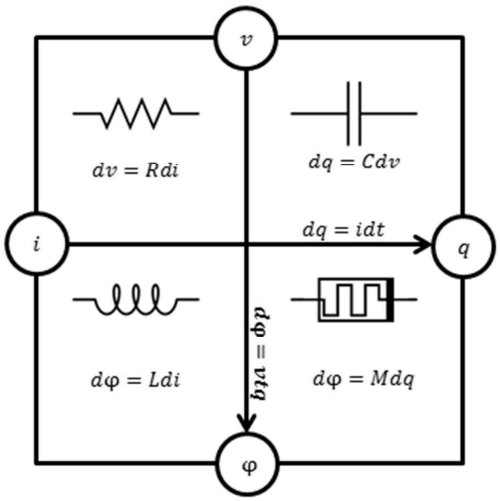
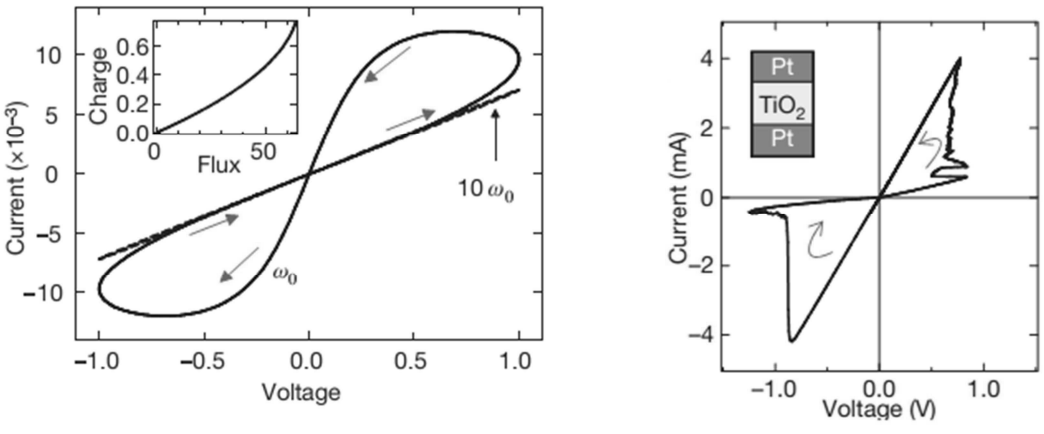



Figure 1: The four fundamental two-terminal circuit elements:
Resistor, Capacitor, Inductor and Memristor.

The memristance relation and definition is:

$$M(q(t)) = \frac{d\phi(q))}{dq} \tag{2.1}$$

Where M is the memristance, q is the charge, $\phi$ is the flux and t is time. The behavior of the memristor is shown in Figure 2 as a relation between the current and the voltage across its terminals. Figure 2 a and b show the theoretical behavior and the actual behavior respectively recorded by HP lab group [1].




(a) (b)

Figure 2: (a) The theoretical behavior (b) The actual behavior recorded by HP lab group.[1]

The difference between the values of the resistances in each state lessens as the frequency applied increases. This causes the memristor to act as a normal resistor at high frequencies depending on the mobility of the dopants in the memristor material [2]. Figure 2 illustrates this phenomenon. This property can be utilized in adaptive filters and frequency dependent circuits.

The memristor is made out of two layers of titanium dioxide ($TiO_2$); one with optimal proportion to each other and the other is with oxygen deficiencies. The two layers are confined between two metals. The thin film is of about a length of 10nm [3]. As the charges flow through it, the oxygen dopants move toward the other layer causing the separating point to move. This movement depends on the amount of flow of charges, the direction of flow and the mobility of the dopants. Figure 3 shows an illustration to the memristor structure.

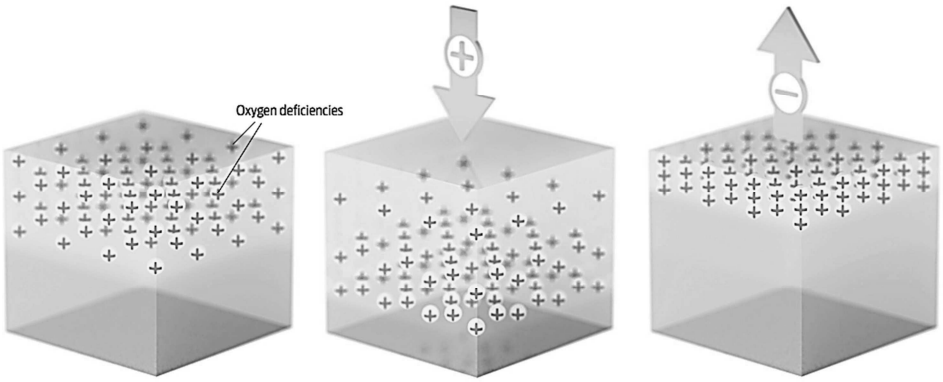



Figure 3: An illustration to the memristor structure [2]

## 1.3. Literature Review

### 1.3.1. Memristor Mathematical Models

Different models have been proposed in the literature for the memristor or any memristive device. Chua in [4] defined the memristive system by the relations shown in equations (2.2) and (2.3).

$$\frac{dw}{dt} = f(w,t) \tag{2.2}$$

$$v(t) = R(w,i) \cdot i(t) \tag{2.3}$$

Where $w$ is an internal state variable describing the location of the barrier between the two layers in the memristor, $v(t)$ is the voltage across the memristor, $i(t)$ is the current passing through the memristor, $R(w,i)$ is the memristance and $t$ is time. Chua also described the characteristics of this system [4] and he proposed different realizations schemes to the memristor [5] which will be presented in the circuit emulators section presented in this thesis. The most important characteristics are the passivity of memristor, no discharge of energy; giving the memristor the non-volatile property working as a memory, symmetry in the v-i characterization curve, the frequency effect on the difference between $R_{ON}$ and $R_{OFF}$ and the difference between applying small AC signal and large AC signal.

Williams in [1] suggested the linear ion drift model describing the drift of the dopants or the oxygen deficiencies. Figure 4 shows a simplified diagram of a memristor equivalent circuit for this modeling of the memristor. The model can be described by the relations in equations (2.4) and (2.5).

$$\frac{dw}{dt} = u_v \frac{R_{ON}}{D} i(t) \tag{2.4}$$

$$v(t) = \left( R_{ON} \frac{w(t)}{D} + R_{OFF}(1 - \frac{w(t))}{D}) \right) \cdot i(t) \tag{2.5}$$

Where $0 < w(t) < D$, D is the distance between the two metal plates, $R_{ON}$ and $R_{OFF}$ are the minimum and maximum values of the memristance respectively, $w(t)$ is the state variable and $u_v$ is the mobility of the dopants.

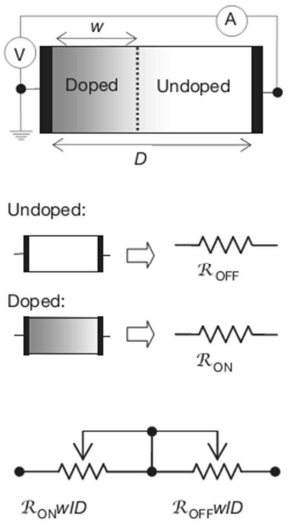



Figure 4: diagram with simplified equivalent circuit for the linear ion drift model

Although William's model [1] satisfies the general behavior of the memristor, the reality showed a highly non-linear behavior [3]. Other mathematical models were also proposed to account for a more accurate behavior from experiments and physics point of view such as Simmon Tunnel Barrier Model and the ThrEshold Adaptive Memristor model, denoted (TEAM) [6]. Only the linear ion drift model did satisfy the memristive system definition although it is the most ideal and yet far from the reality [6]. Using the mathematical models one can understand the behavior and simulate applications but it does not account for all parameters. Different characteristics are required for different

applications. To have practical imitation to the behavior of a memristor in different applications, an emulator is needed to verify a proper operation.

### 1.3.2. Memristor Circuit Emulators

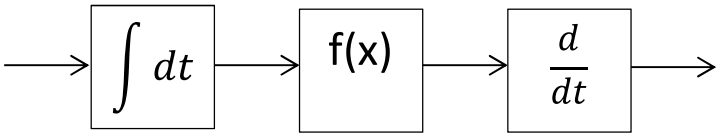
The circuit emulator is a circuit built around commercially available integrated circuits and electronic devices. Due to the unavailability of a memristor sample, this approach is needed to implement memristor based applications. Also, it is highly unlikely that the manufacturer companies will provide a two terminal memristor but rather integrated circuits with many memristors in certain application such as in RAMs.

When implementing such emulators and incorporating them in an application, one has to take care of some aspects and criteria. Such as controllability over the values of $R_{ON}$ and $R_{OFF}$, which for practicality will be called $R_{LOW}$ and $R_{HIGH}$, or whether there are more discrete states for the memristance value. Some applications require continuous state level especially for analog applications such as oscillators. An important factor is the speed of transition between $R_{LOW}$ and $R_{HIGH}$ which need to be considered as well. Also, the loading interface of the circuit emulator is very crucial when interfacing the circuit emulator in an application with other circuits. If the memristor is going to be fed from an output current of another circuit then the input resistance of the memristor emulator has to be much lower than the output resistance of the feeding circuit and the opposite goes for voltage signals. Another aspect is the energy discharge or the phase between the voltage applied and the current passing through. For a memristor, the phase has to be zero for it to act as a resistor according to the characteristics described by Chua in [4]. Chua also described the memristor to have a symmetrical v-i Lissajous curve [4]. Aside from the grounded memristor emulator, there is a need for a floating memristor

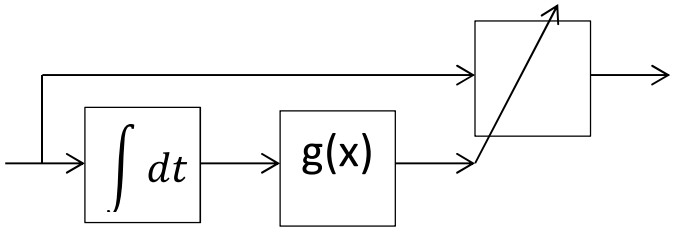
emulator in many applications. Controlling the direction of charging the state level of the memristor is needed in applications such as in relaxation oscillators. The direction of charging is whether it is incremental or decremental, that is the value of the memristance is increasing or decreasing with the direction of current. Another property of the memristor is the non-volatility of the memristance value. That is the value of the memristance does not revert to an original state but keeps the last state it reached upon passage of charges.

Many memristor emulators have been introduced in the literature [7]-[15]. They can be divided into two groups; Analog memristor emulators and digital or hybrid memristor emulators [16]. The analog circuit emulators or mutators, as it is named by some authors, follow two general methods. The first is applying what Chua presented in his work [5] that is modeled in Figure 5 (a). This approach operates by integrating the input variable which can be either voltage or current to have the flux or charge value respectively. Then applying the non-linear operation f(x) which will decide the behavior of the memristance then differentiating the state variable back to voltage or current. The function f(x) is where the memristance can have the incremental or decremental property. Also, it will decide the values for $R_{LOW}$ and $R_{HIGH}$ or whether there are more states for memristance than only these two values and whether the memristance has discrete or continuous levels. This method follows the definition of the memristor and can acquire most of the fingerprints of the memristor except the non-volatility and, depending on the design, the odd-symmetry of the v-i curve might be affected. The work in [7] and [10] follows the model described in Figure 5 (a). The second method in modeling analog memristor emulator is described in Figure 5 (b) where the input variable being voltage or

current is integrated to get the state variable being the flux or the charge. Then the function g(x) is applied to the state variable resulting in a coefficient that will control the amount of output variable in terms of the input variable. The controlling circuit is usually a multiplier circuit like in [9], [11] and [12]. In the work reported in [8], they used a light dependent resistor LDR as their controlling circuit while the work in [13] utilize a junction field effect transistor JFET as a controllable resistance for the controlling circuit. The limitation of this method will be mainly on the controlling circuit. Both models uses an integrator before the scaling function to have a 90 degrees phase shift then treating the positive half of the shifted signal differently from the negative half to achieve the special v-i characteristics. The integrator also will attenuate high frequency signals. This will reduce the difference between the treatments, of the positive and negative halves, in low frequency signals and high frequency signals. This is one of the fingerprints of the memristor that it does tend to behave as a normal resistor as the frequency increases.




(a)




(b)

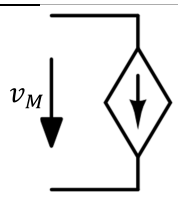
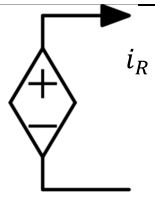
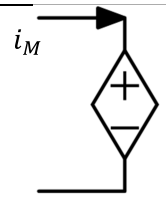
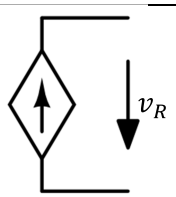
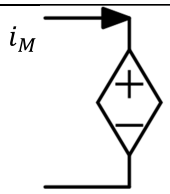
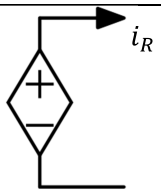
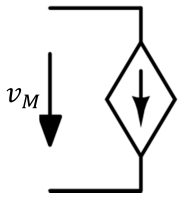
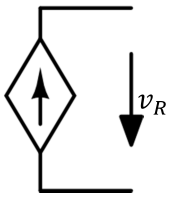
Figure 5: Analog emulator general models [16]

The digital or hybrid approach in memristor emulation is described in [14]-[15]. This approach have the advantage of having a non-volatile memristor emulator but it is

more complicated and uses a digital controller such as micro-controllers as the heart of the circuit. The work in [14] uses a microcontroller to read the voltage applied between two points through an analog to digital block and then control a programmable variable resistance to control the current passing between these two points. Thus acquiring the behavior required which is programmed in the microcontroller. The work in [15] uses a microcontroller to read the voltage from an analog to digital block and then controlling a current source circuit using a digital to analog converter.

Chua showed in [5] different realizations of the memristor using controlled sources as shown in Table 1. The table follows the approach described in Figure 5 (a). There are four approaches which are categorized as realizations 1 and 2. In each realization there are two types. The variables on the left side of the figure of each approach are the voltage across the memristor and the current passing through the memristor. The variables on the right hand side are the voltage that will be applied on a non-linear resistor and the current passing through it. The non-linear resistor will decide the behavior of the function f(x) in the model Figure 5 (a). The table shows all possible combinations and relations between the voltages and currents $V_M$, $I_M$, $V_R$ and $I_R$. Depending on the location of the circuit and the configuration of the non-linear resistors used, it can be decided which approach to take.

Table 1: Characherization and realizations of the memristor mutator [7]

| Type | Realization 1 | | Realization 2 | |
|---|---|---|---|---|
| 1 |  |  |  |  |
| | $i_M = k_y \frac{di_R}{dt}$ | $v_R = \frac{1}{k_x}\int v_M dt$ | $v_M = k_x \frac{dv_R}{dt}$ | $i_R = \frac{1}{k_y}\int i_M dt$ |
| 2 |  |  |  |  |
| | $v_M = k_y \frac{v_R}{dt}$ | $v_R = \frac{1}{k_x}\int i_M dt$ | $i_M = \frac{dv_R}{dt}$ | $i_R = \frac{1}{k_y}\int v_M dt$ |

The work done in [7] is based on type 1 of realization 1. The memristor circuit emulator used is shown in Figure 6. The integrated circuits 1 and 2 are current feedback operational amplifiers CFOAs while 3 is an OPAMP. This circuit emulator is good in mutating the general behavior of the memristor as a binary state resistor. Also, the level of $R_{LOW}$ and $R_{HIGH}$ can be controlled by changing the values of $R_1$, $R_2$ and Rd. The circuit mutates the q-ϕ relation of the memristor using two resistors, two capacitors, a non-linear resistor with an operational amplifier and two current feedback operational amplifiers. The non-linear resistor is used to emulate the bow-tie relation in the i-v curve which will give us two discrete values for the state levels making this emulator suitable for binary operations.

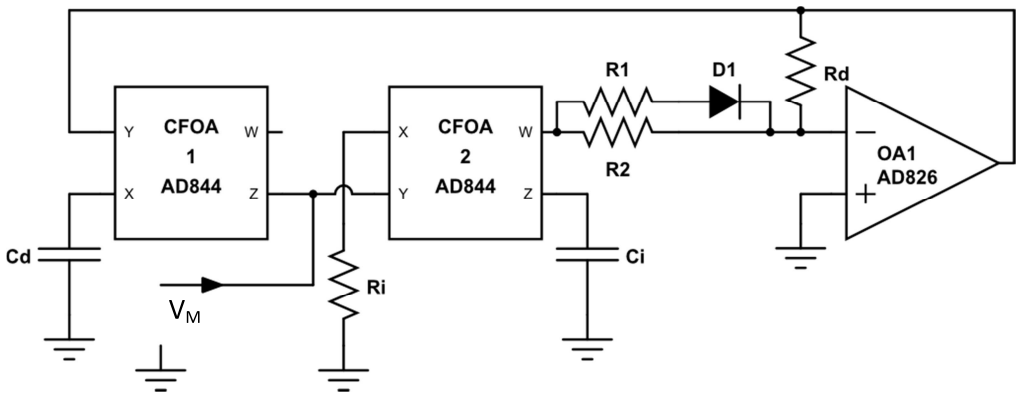



Figure 6: Circuit emulator proposed by [7]

The circuit, in Figure 6, is operating to satisfy the characteristic equations and relations between the charge through the mutator and the flux linkage as it explained by equation (2.6) and (2.7). The input voltage signal will be integrated and then scaled through the non-linear resistor with the amplifier to treat the positive half of the signal differently than the negative half. The output signal of the non-linear scalar is then differentiated to have the current ($i_M$) as needed. In this circuit, the voltage applied ($v_M$) will induce a current through $R_i$. This current will be integrated in the capacitor $C_i$ giving a voltage at the w node of the CFOA2. The non-linear resistor will scale this voltage in the negative gain OPAMP based amplifier. The voltage out of the amplifier will be differentiated in the capacitor $C_d$ inducing the current $i_M$.

$$v_c = \frac{1}{R_i C_i} \int v_M dt \tag{2.6}$$

$$i_c = R_d C_d \frac{d}{dt} i_R \tag{2.7}$$

Equations (2.6) and (2.7) show the relation between $v_c$-$v_M$ and $i_c$-$i_R$. These parameters are related by the non-linear resistor to have two different slopes in the i-v curve. The non-linear resistor has been realized by connecting a light emitting diode in series with a resistor and shunting the end terminals by another resistor as shown in

Figure 7. This configuration can be done as well using a normal diode taking into consideration the difference between the forward bias voltage of the normal diode and the LED.

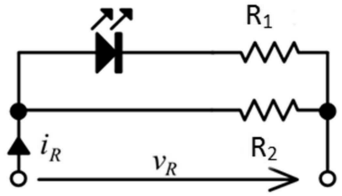



Figure 7: Implementation of the non-linear resistor

The circuit was implemented using $R_i$ and $R_d$ as 4.7kΩ, $C_i$ and $C_d$ as 47nF, $R_1$ as 1.2kΩ and $R_2$ as 2.4kΩ. The two capacitors were shunted by 47kΩ resistors. The current was probed by converting the differential voltage across a 10Ω series resistor using an instrumentation amplifier with gain 47. Figure 8 (a) and (b) show the best performance for the circuit at 1 KHz. The LED used in the non-linear resistor has a forward voltage of 0.91V.

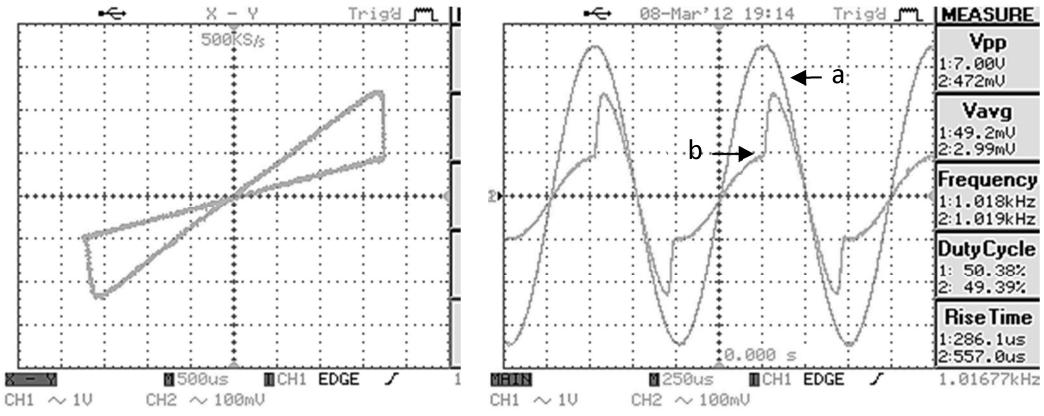



Figure 8: (a) i-v curve of the mutator at 1 KHz. (b) The mutator voltage (a) and current (b) vs. time.

The circuit emulates the memristor behavior at low frequencies and it is suitable for a voltage driven memristor. However, the OPAMP at relatively high frequency will

introduce a pole which can have an effect on the behavior of any external circuit if used in an application. This limits the frequency bandwidth of the applied signal if used in analog applications as will be discussed later in this thesis. Also, due to the internal resistance of the Z-terminal of the CFOA used, the behavior is affected causing a shift in the v-i curve and, more significantly, it will discharge the charge accumulated on the capacitor Ci. This will force the memristor to lose the state level after a period of time depending on the output resistance of the CFOA and the capacitance Ci.

As a memristor, the behavior of this mutator changes as the frequency increases. This realizes the memristance vs. frequency relation of the memristor. Experimental results show that as the signal frequency applied across the memristor increases, the memristor starts to behave as a normal single valued resistor. This phenomenon is shown in Figure 9 for the design of the grounded memristor and adding a constant voltage on the positive terminal of the operational amplifier for better frequency range.

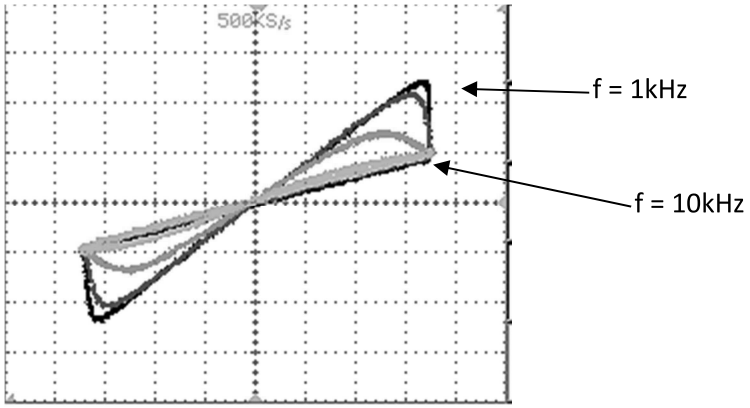



Figure 9: Experimental i-v curve of the mutator with different frequencies (from 1 KHz to 10 KHz)

The circuit shown in Figure 10 was proposed by [10]. It follows type 2 realization 1 shown in Table 1. The circuit uses a current follower with two outputs, a positive type

second generation current conveyer, a capacitor, and inductor and a non-linear resistor as shown in the figure. The mutator is driven by a current and the output parameter is the memristor voltage. The work is based on computer simulation. The current input will be integrated through the capacitor C1 and the voltage across the capacitor will drive the non-linear resistor. The current passing through the non-linear resistor will be buffered through the current follower to be differentiated in the inductor L1 as a voltage. The voltage across the inductor will be buffered back to the X terminal of the CCII+ block and to the terminal of the memristor mutator. The circuit was designed poorly ignoring the current that will pass from the Z terminal of the CCII+ to the non-linear resistance. A voltage buffer is needed between the capacitor and the non-linear resistor. Also, the second output of the current follower should not be fed back through the non-linear resistor to the input of the current follower. Using an inductor in the Z terminal of the current follower is risky since it can short the output buffer of the current follower upon saturation or if a DC signal was applied on the terminals of the emulator.

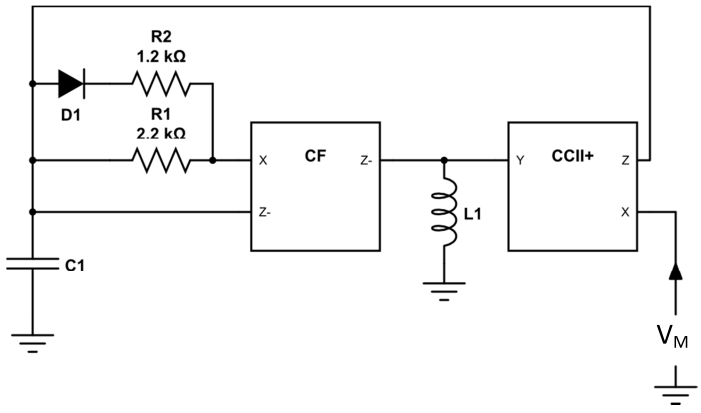



Figure 10: circuit emulator proposed by [10].

Another circuit emulator was proposed in [8], shown in Figure 11, uses the general model in Figure 5 (b). The emulator uses only operational amplifiers, resistors

and uses an LDR to control the current produced as a function of the input voltage. The emulator will realize binary state levels for the memristor. The circuit is driven by voltage and the controlled variable is the current. The input voltage will be buffered and inverted to an integrator circuit. The output of the integrator is then added with a constant in OA3 circuit which is then driving the nonlinear resistor. The nonlinear resistor will drive the LDR either to be ON or OFF thus having two values for the resistance, LOW and HIGH. The values reported were between 483.606Ω to 688.610Ω. As it stands, this circuit is not suitable placing it in any application since the loading interface has to be accounted for. Also, the frequency is limited by the operational amplifier. The LDR is causing a significant limitation to the current since it is used as a simple variable or controlled resistance. This will affect the loading interface as well.

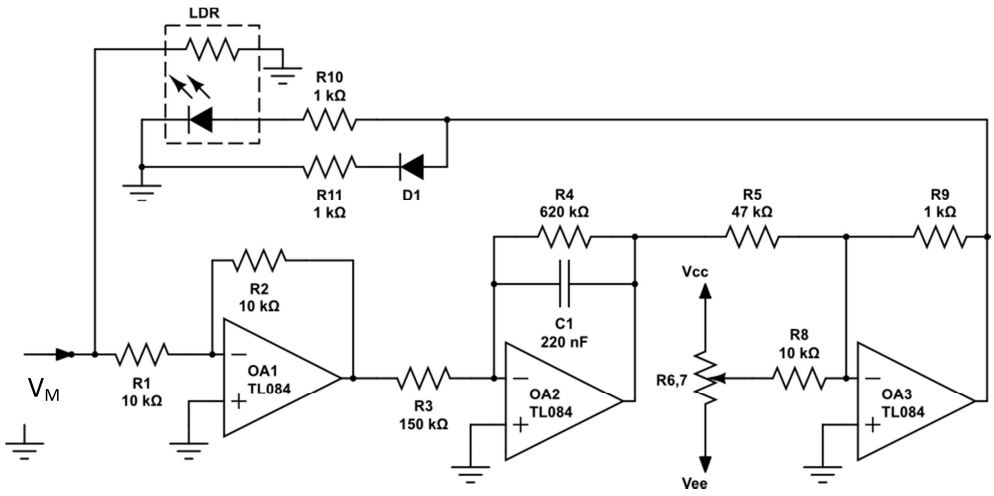



Figure 11: Circuit emulator proposed by [8]

The work in [9], shown in Figure 12, is claimed to mimic the behavior of a floating memristive system. The circuit operated as explained in Figure 5 (b). It uses two operational amplifiers with a multiplier circuit. U1 and U2 are OPAMPs circuits and U3 is a multiplier circuit (AD633JN). The function equation of the multiplier is given in

equation (2.8) [17]. The first OPAMP will amplify the voltage across the memristor and the second OPAMP will integrate that voltage. The multiplier circuit will multiply the output of the integrator with the input voltage. The output should have been converted to current or used to control the current output from node B. Also, the current from the terminal w of the multiplier circuit cannot be determined. The circuit is claimed to be floating however the current from one terminal is not equal to the current in the second terminal. However, the author pointed out this issue in his work as well. As it stands, this circuit is not suitable as well for placing it in an application since the loading interface has to be accounted for. Also, the frequency is limited by the operational amplifiers.

$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z \tag{2.8}$$

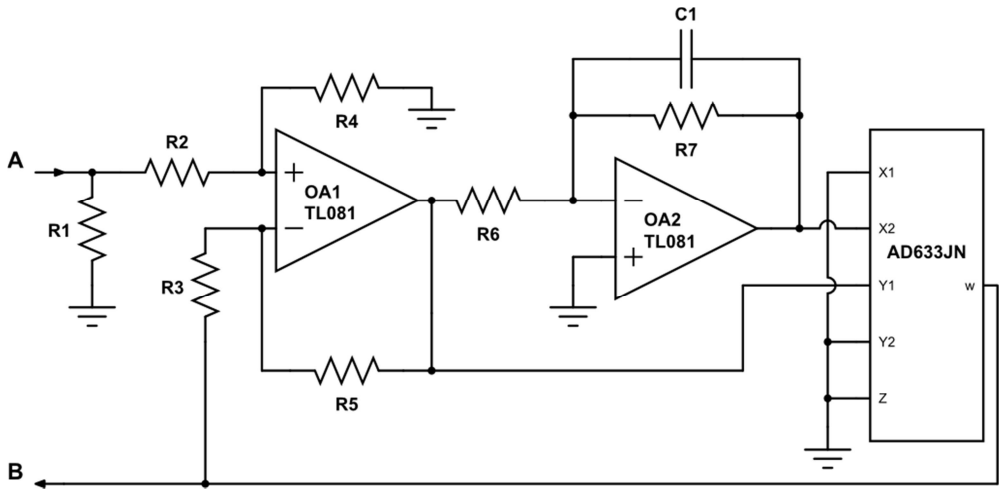



Figure 12: Circuit emulator from [9]

The circuit emulator reported in [11] uses a complex circuit that contains ten MOSFET transistors with four OPAMPS and a multiplier IC along with resistors and a capacitor. The circuit follows the approach explained in Figure 5 (b). The circuit is not suitable to be used as two terminal memristor in an application because of its complexity

and the input resistance restrictions. The circuit is driven by voltage and the controlled variable is the current. Another circuit reported in [12] uses the same approach as in Figure 5 (b) with a modification that the state variable after integration is squared then multiplied by the input parameter that is the voltage in this case. The output is then converted to current by using an OPAMP circuit. The circuit uses three OPAMPs, two multipliers and some passive components. The circuit is driven by voltage and the controlled variable is the current. The circuit does not follow the original definition of the memristor but it does mimic a memristive system behavior. Another circuit was report in [13] that follows the same approach as in Figure 5 (b). It uses five OPAMPs with many passive components. The circuit uses a JFET transistor to control the output parameter which is the current in this case. The circuit has a poor input interface and it uses many active and passive elements.

An overall view of the reported memristor emulators shows that they suffer from one or more of the following drawbacks:

1. The use of inductors which is not desirable in integration [10].
2. Additional interfacing circuits are needed if it is to be used as a two terminal device in an application [8]-[9], [11], [13].
3. The emulator is voltage driven only which limits its possibility to be used in current driven circuits [7]-[9], [11]-[13].
4. The use of digital and analog circuits [14]-[15].

A comparison table for all reported memristor emulators is given in Table 2.

Table 2: Comparison table between the reported circuit emulators

| *Criterion for comparison* | **[7]** | **[10]** | **[8]** | **[9]** | **[11]** | **[12]** | **[13]** |
|---|---|---|---|---|---|---|---|
| **Control variable** | Voltage | Current | Voltage | Voltage | Voltage | Voltage | Voltage |
| **Input resistance** | High | Low | Relatively High | Relatively High | Relatively High | Relatively High | Relatively High |
| **Interface with other circuits** | good | good | bad | bad | bad | Good | bad |
| **Symmetric Lissajous Figure property** | No | No | No | Yes | Yes | Yes | Yes |
| **Floating** | No | No | No | Yes* | No | No | No |
| **Discrete (D) state levels vs. Continuous (C)** | D | D | D | C | C | C | C |
| **Direction of change of memristivity** | Single | Single | Single | Single | Single | Single | Single |

*however the current from one terminal is not equal to the current in the second terminal

### 1.3.3. Memristor Applications

Several analog application circuits have been proposed in the literature that base their operation on the Memristor behavior. Most of the applications are based on the change of the memristance with the voltage integration over time. Such applications include multi-vibrating oscillators [18][19], modulation of signals i.e. AM, ASK, FSK and BPSK[20][21][22], chaotic oscillators[23], sinusoidal oscillators[24] and analog memory [25][26][27].

The memristor has the property of a changing resistance with the passage of current. However, from the physics point of view, the oxygen deficiencies' movement is limited in speed or transition. This transition is bounded by the parameter μv that is the

mobility of the dopant movement. Rewriting equation (2.1) in terms of current will lead to equation (2.9). If a sinusoidal signal is applied, the factor $1/\omega$ will appear as in equation (2.10). So as the frequency increases, the difference between the maximum resistance and the minimum resistance will decrease.

$$v(t) = M\left(\int_0^t i(\tau)d\tau\right) i(t) \tag{2.9}$$

$$v(t) = M\left(\frac{1}{w} I_o sin(wt)\right) I_o cos(wt) \tag{2.10}$$

This is exploited in the modulation applications such that when applying a small signal, faster than the movement of the dopants, the state level of the memristor will not move or will move insignificantly. So it can be used as if there are two signals added together. One that will be the message signal and one will be a controlling signal. The carrier is a sinusoidal high frequency signal with no DC component and the message will be a low frequency signal so that it does control the memristance. The message signal can be pulses or any value such that the integration of the current over a certain period of time is what will determine the new memristance level. The level changes with relation to the amplitude of the current injected and the time period of applying the current. Refer to Figure 2 (a) for an illustration of this behavior. Note that the memristance cannot exceed the boundary values of $R_{ON}$ and $R_{OFF}$.

The work done in [21] takes advantage of these properties. The proposed circuits simulated are shown in Figure 13 for an amplitude-shift-keying modulator using single memristor, Figure 14 for a frequency-shift-keying modulator using two memristors and Figure 15 for a binary-phase-shift-keying modulator using two memristors. The work assumes two values of memristances where $R_{LOW}$ is much smaller than $R_{HIGH}$. A

preprocessor circuit is needed as the control signal that will control the state level of the memristor. This can be just a series of pulses where the number of pulses and their polarity will control the memristor level. A DC signal will suffice if the memristor has only two levels. The message signals are currents while the outputs are voltages.

For Figure 13, if the memristance is at $R_{LOW}$ value, the output voltage will be very small relative to the voltage when the memristance is at $R_{HIGH}$. So by controlling the level of the memristance, different amplitudes can be achieved thus having an ASK modulation.

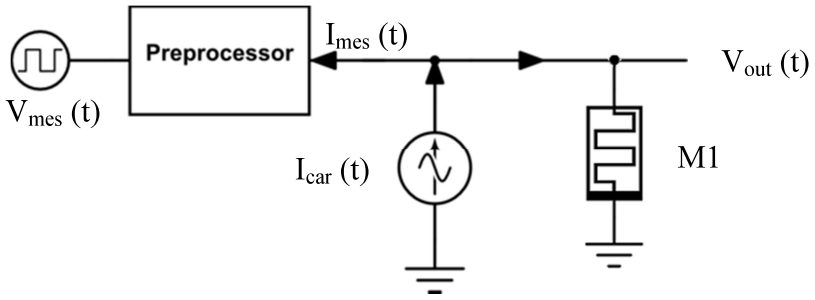



Figure 13: An amplitude-shift-keying modulator using single memristor [21]

For Figure 14, the same principle is used but with using two sources with different frequencies and two memristors. The memristors M1 and M2 must be at opposite levels so that either the effect of the first source will be in the output or the effect of the second source will be in the output. A third configuration is when both M1 and M2 are set to $R_{LOW}$ which will lead to turning the output off. The preprocessor circuit will control the levels of M1 and M2.

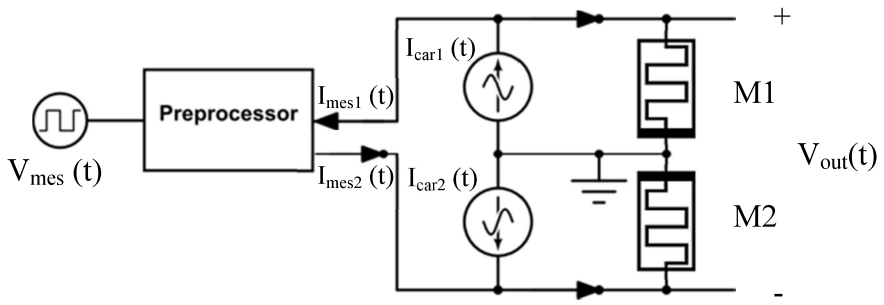



Figure 14: A frequency-shift-keying modulator using two memristors [21]

For Figure 15, a single source is used with two memristors. The memristors M1 and M2 must be at opposite levels as well and the polarity of the output voltage will change thus giving a 180 degree shift in phase. If M1 is at $R_{HIGH}$ value, M2 will act as a short circuit thus the phase output will be at 0 degree phase with the input signal. If M2 is at $R_{HIGH}$, M1 will act as a short circuit and the phase of the output will be at 180 degrees phase shift with the input signal, producing a BPSK modulation.

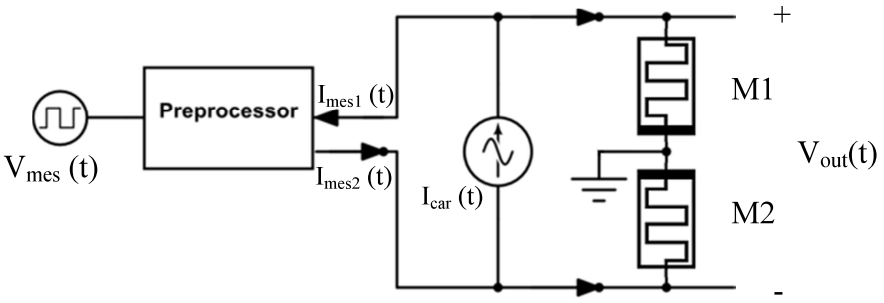



Figure 15: A binary-phase-shift-keying modulator using two memristors [21]

The work in [20] is an application of using the memristor in filters taking to advantage the reconfigurable property of the memristance. Results of this work are shown in Figure 16 for a low pass filter and a high pass filter.

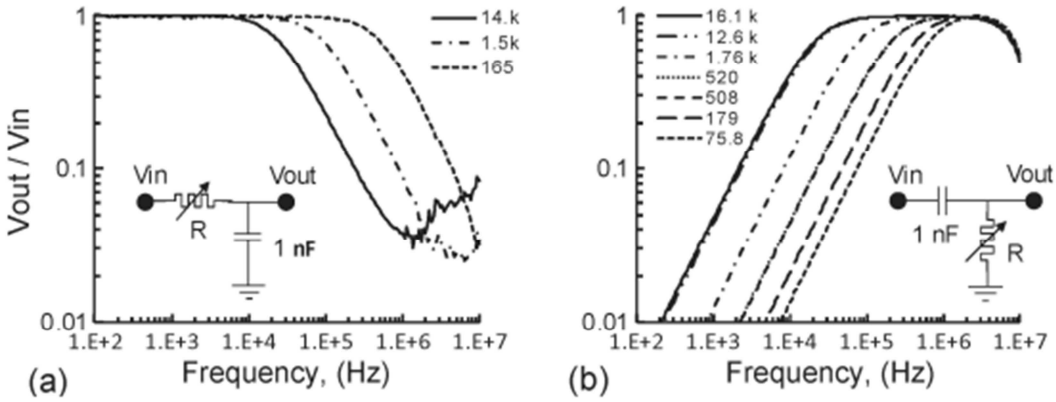



Figure 16: a LPF and a HPF implemented by [20] showing the tunability of the memristance with the change in the corner frequency of the filters

For the sinusoidal oscillator reported in [24], the memristor was used by replacing the resistances in the circuit. Analysis of the oscillator was carried out to incorporate the memristance change in the response and the condition of oscillation. The work was based in the famous Wien-bridge oscillator shown in Figure 17.

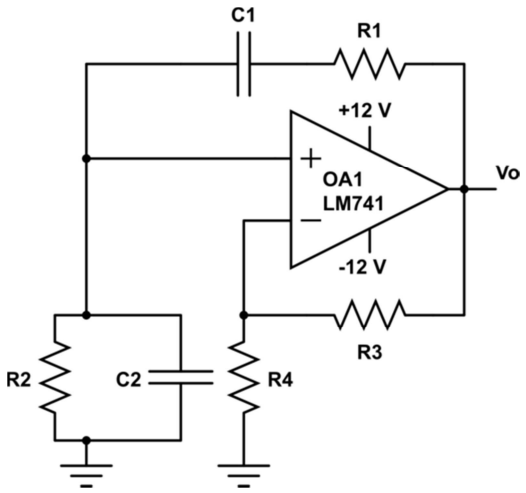



Figure 17: Wien bridge oscillator circuit with possibility of replacing resistor with memristors

## 1.4. Problem definition

The different emulators in the literature can give a memristive behavior but it cannot necessarily accommodate applying it in any application. There are different parameters that have to be considered. Also, different applications might require different emulators. For example, in a digital application, the difference between $R_{LOW}$ and $R_{HIGH}$ must be high and the transition has to be fast thus the binary emulator has to be used. These considerations have been explored and different emulators have been proposed and tested. Such consideration includes the input loading, grounded and floating memristor configuration, incremental or decremental behavior and the number of state level for the memristance and possibly for future applications that might need a memristor with negative memristance.

Different applications of the memristor have to be explored using the proposed emulators. The behavior of the memristor in these applications has to be observed. A search for new applications or improved implementations to old applications is desired.

## 1.5. Thesis Organization

Chapter 2 will discuss different proposed emulators for the memristor with different properties. In Chapter 3, some applications to the proposed emulators will be shown based on experimental results. Then Chapter 5 will conclude this thesis.

# Chapter 2

# Proposed Emulators

The work done in this thesis is based on the emulator proposed in [7] and shown in Figure 6 with some enhancements and manipulations. This emulator was chosen because it is the closest to the memristor behavior following the characteristics equations as of [4] and for its simplicity. The realization of the emulator is explained in Table 1 as type 1 realization 1. The use of the OPAMP introduces a pole at high frequency depending on the gain because of the limitation of the gain-bandwidth product. Also, the forward voltage of the diode will introduce a voltage shift thus will affect i-v characteristics curve for the overall circuit. Moreover, to achieve high gain amplifier using the OPAMP which will help to increase the ratio between $R_{LOW}$ and $R_{HIGH}$, the ratio between the feedback resistance and the input resistance has to be high thus there is a need for high values of resistance in the feedback to have good input resistance and good gain.

The non-linear scalar, of Figure 18, is proposed to have different gains at different polarities after the integrator. This part of the circuit is responsible for the number of state levels for the memristor. Here we have only two states making this circuit suitable for binary operation such as digital operations or in binary switching for analog applications as well. To overcome these disadvantages of the circuit, a CFOA is replacing the OPAMP circuit as shown in Figure 18. This circuit is an inverting amplifier in the condition that $R_d$ is smaller than $R_{eq}$, where $R_{eq}$ is the effective resistance between points a and b. The gain is given by equation (3.1). The gain for this circuit must be negative

because an inverting amplifier is needed to satisfy the emulator behavior. From the gain equation, it is clear that there is no need for high value of resistances to get high gain but rather the difference between $R_{eq}$ and $R_d$ must be as small as possible and must be positive. The voltage at node a is the input voltage while the voltage at point b is the output voltage. Since those two voltages have different polarities, this will increase the voltage difference across the diode thus it will allow for a current to pass through the diode even if the input voltage (Vin) is less than the forward voltage of the diode. This is true with the condition that the gain is negative when the diode is turned off as shown in equation (3.3). This is clear from the characteristics curve of the amplifier shown in Figure 19 (a) where the gain with the diode off is approximately -1.3. The input voltage at which the diode will turn on using equation (3.3) is equal 0.13V assuming a forward voltage of 0.3V. Figure 19 (a) and (b) show the overall characteristics of the amplifier using R1= 18kΩ, R2=9.1kΩ, Rd=5.186kΩ and using a germanium diode D1.

$$Gain = \frac{V_o}{V_{in}} = \frac{-R_d}{R_{eq} - R_d} \tag{3.1}$$

where $R_{eq} = \begin{bmatrix} R_2 & ,if\ the\ diode\ is\ off \\ R_1//R_2 & ,if\ the\ diode\ is\ on \end{bmatrix}$ and $R_{eq} > R_d$. The voltage between a and b where the diode will start passing current can be approximated as

$$V_a - V_b \approx V_f \tag{3.2}$$

where $V_f$ is the forward voltage of the diode.

From equation (3.1) and (3.2),

$$V_{in} \approx \frac{V_f}{1 - Gain_{\ with\ the\ diode\ off}} \tag{3.3}$$

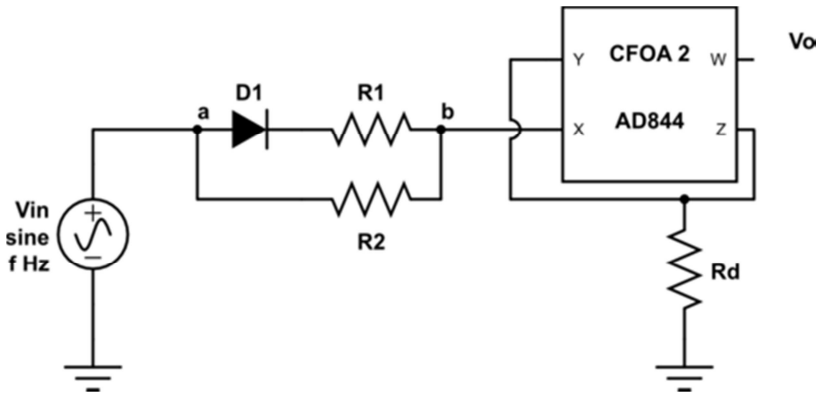
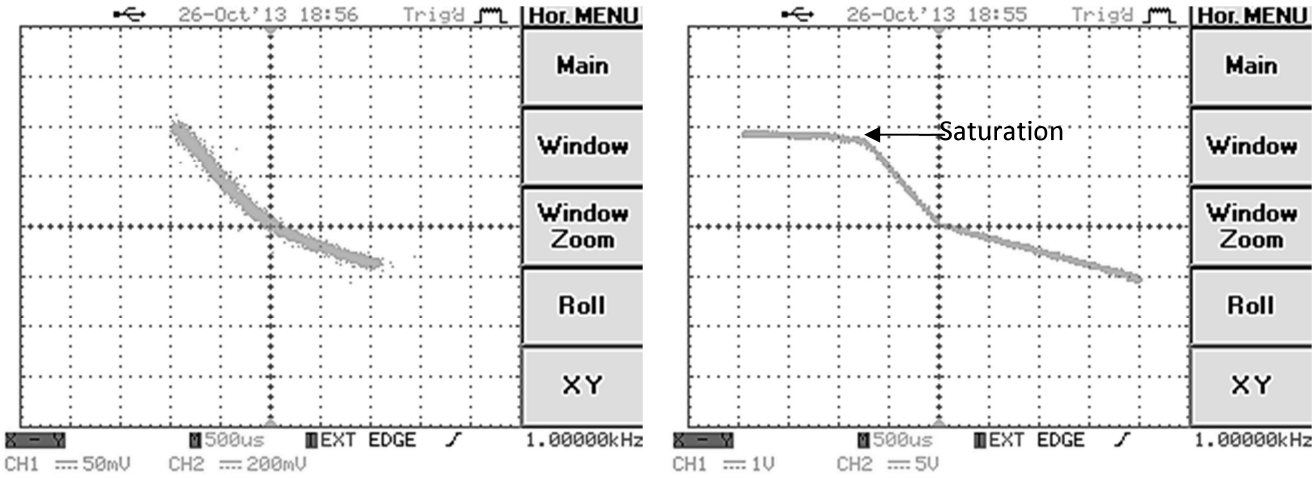


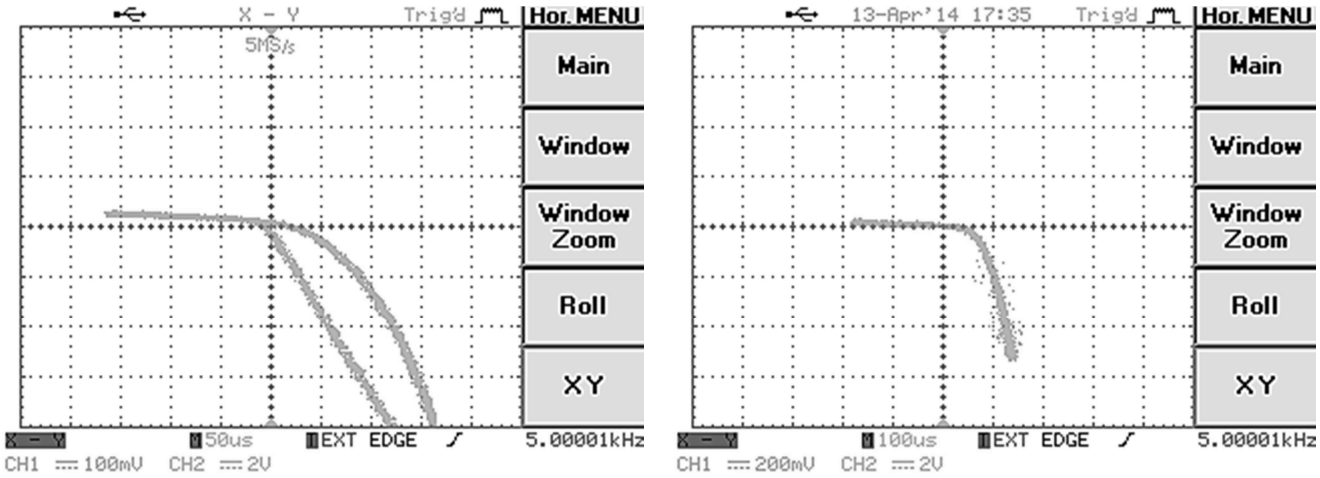

Figure 18: The non-linear scalar proposed




(a) (b)

Figure 19: The characteristics curve of the amplifier Vo vs. Vin with (a) Vin = 200m$V_{p-p}$ (b) Vin = 8$V_{p-p}$

Figure 20 shows the characteristics curve, $V_o$ versus $V_{in}$, at a frequency of 5 kHz and the high gain part of the curve has a gain of approximately 37 for both circuits. Inspection of Figure 20 shows that the performance of the OPAMP-based emulator has a hysteresis in the characteristic which will affect the performance of the emulator as a memristor. This can be attributed to the limited gain-bandwidth product of the OPAMP. However, the CFOA-based realization does not show this hysteresis. This confirms the usefulness of using the CFOA instead of the OPAMP especially at high frequency.




(a) (b)

Figure 20: The characteristics curves Vo vs. Vin at f=5 kHz with the same maximum gain value of (a) the non-linear scalar circuit reported in [7] and (b) the non-linear scaler propsed.

## 2.1. New design based on CFOA only with different input impedance option for better loading

The designs of Figure 21 and Figure 22 take advantage of using CFOA for all the integrated circuits. This will remove the limitations shown of using the OPAMP. The circuit of Figure 21 is suitable for voltage driven memristor as it enjoys high input resistance. The circuit of Figure 22 is suitable for current driven memristor as it enjoys low input resistance. In Figure 21, the voltage will be sensed from a Y-terminal and the current related with this voltage by the memristance characteristics will be supplied from a Z-terminal. As for Figure 22, the current will be sensed from the X-terminal and the voltage related to that current by the memristance characteristics will be on terminal X as well buffered from the Y-terminal of that CFOA. These circuits have two state levels.

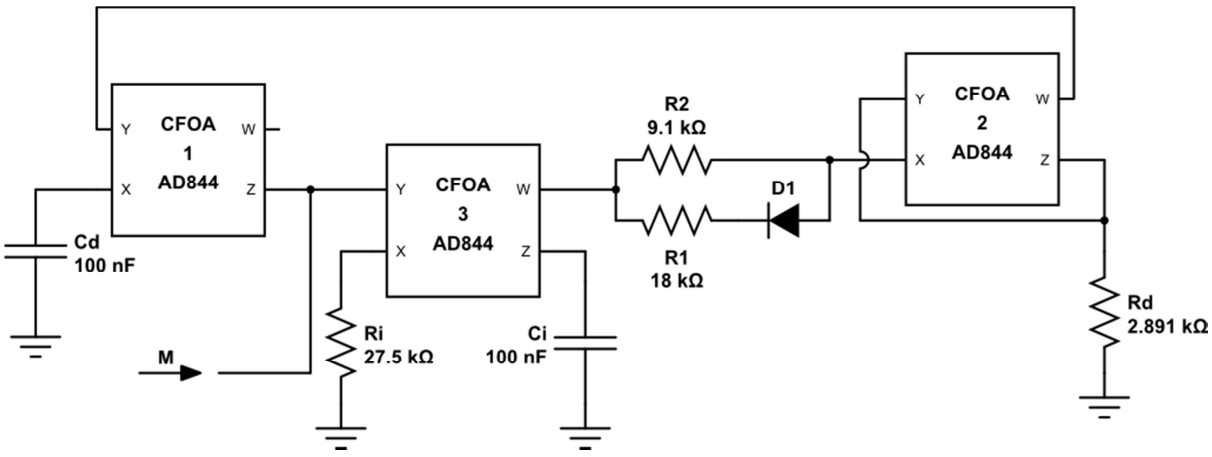



Figure 21: New memristor circuit emulator with high input impedance

The circuit of Figure 21 follows type 1 realization 1 from the different approaches shown in Table 1. The characteristics equations for the emulator are given in equation (3.4) and (3.5). The current $I_R$ equation is given in (3.6). Equation (3.7) shows the overall memristance that the circuit will have with the condition that $R_d$ must be less than $R_{eq}$ to have a positive memristance. The memristance will have two values depending on the value of $R_{eq}$ which depend on the diode state.

$$V_R = \frac{1}{R_i C_i} \int V_M dt \tag{3.4}$$

$$I_M = R_d C_d \frac{d}{dt} I_R \tag{3.5}$$

$$I_R = \frac{V_R}{R_{eq} - R_d} \tag{3.6}$$

Dividing $V_M$ by $I_M$ from equation (3.4) and (3.5),

$$M = \frac{(R_{eq} - R_d) R_i C_i}{R_d C_d} \qquad , R_{eq} > R_d \tag{3.7}$$

where $R_{eq} = \begin{bmatrix} R_2 & ,if\ the\ diode\ is\ off \\ R_1//R_2 & ,if\ the\ diode\ is\ on \end{bmatrix}$, $V_R$ is the voltage at node w of CFOA3, $I_R$ is the current passing through the non-linear resistor, $V_M$is the voltage at the input of the memristor, $I_M$ is the current passing through the memristor and $M$ is the memristance.

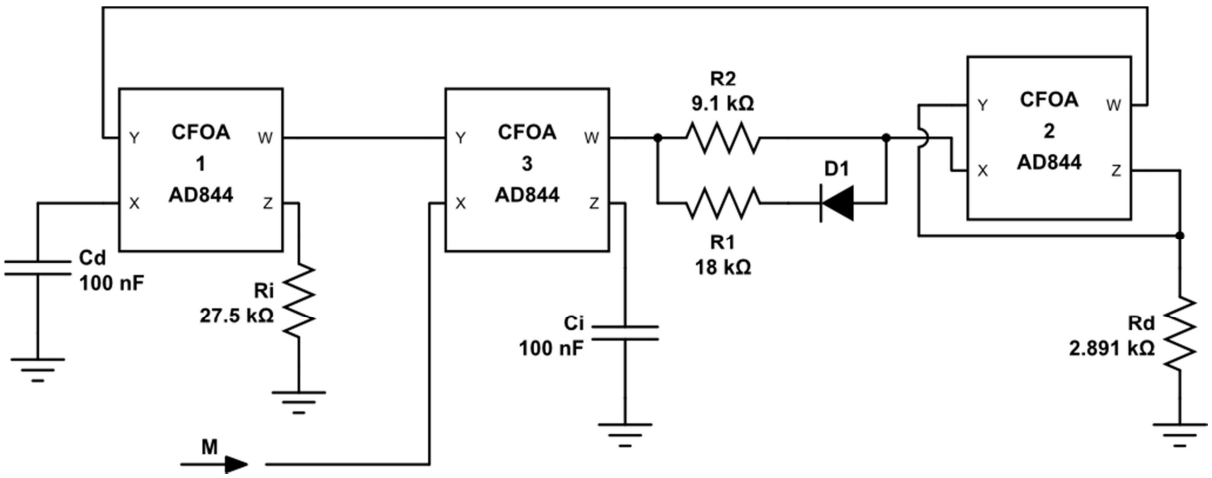



Figure 22: Memristor circuit emulator with low input impedance

The circuit of Figure 22 follows type 2 realization 1 from the different approaches shown in Table 1. The characteristics equations for the emulator are given in equation (3.8) and (3.9). Equation (3.10) shows the overall memristance that the circuit will have with the condition that $R_d$ must be less than $R_{eq}$ to have a positive memristance. The memristance will have two values depending on the value of $R_{eq}$ which depend on the diode state.

$$V_R = \frac{-1}{C_i}\int I_M dt \tag{3.8}$$

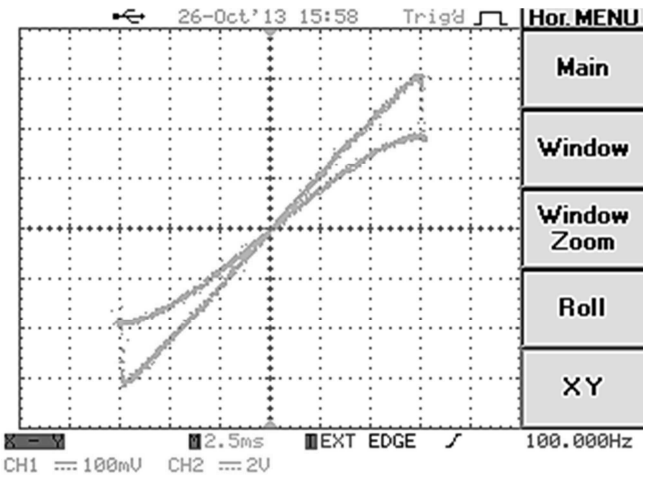
$$V_M = \frac{-R_i R_d C_d}{(R_{eq} - R_d)}\frac{d}{dt}\ V_R \tag{3.9}$$

Dividing $V_M$ by $I_M$ from equation (3.8) and (3.9),

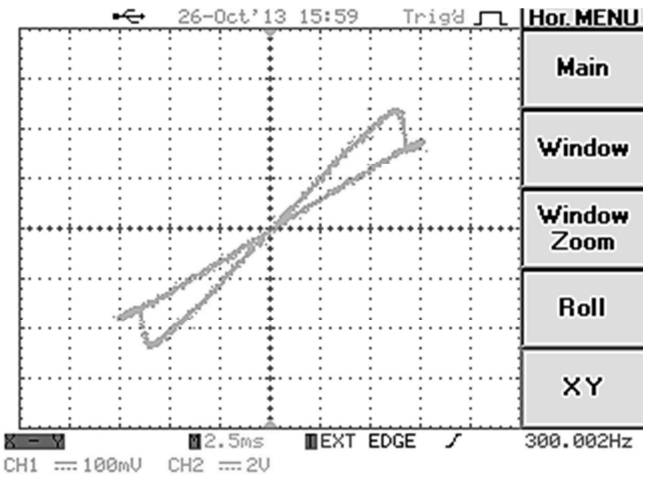
$$M = \frac{R_d C_d R_i}{(R_{eq} - R_d)C_i} \qquad , R_{eq} > R_d \tag{3.10}$$

where $R_{eq} = \begin{bmatrix} R_2 & ,if\ the\ diode\ is\ off \\ R_1 // R_2 & ,if\ the\ diode\ is\ on \end{bmatrix}$

The circuits has been tested and implemented in different applications. In order to test the functionality of Figure 22, the input current was obtained from the Z-terminal output of a CFOA fed from a function generator in the Y-terminal with a resistor from the X-terminal to ground. Figure 23 (a-d) show the v-i characteristics of Figure 22 obtained at different frequencies. Figure 23(e) shows the waveforms obtained for the current through and the voltage across the memristor. Figure 23(f) shows that at relatively high frequency, the memristor state level is not changing or has a negligible change as equation (2.10) indicates.




(a)




(b)

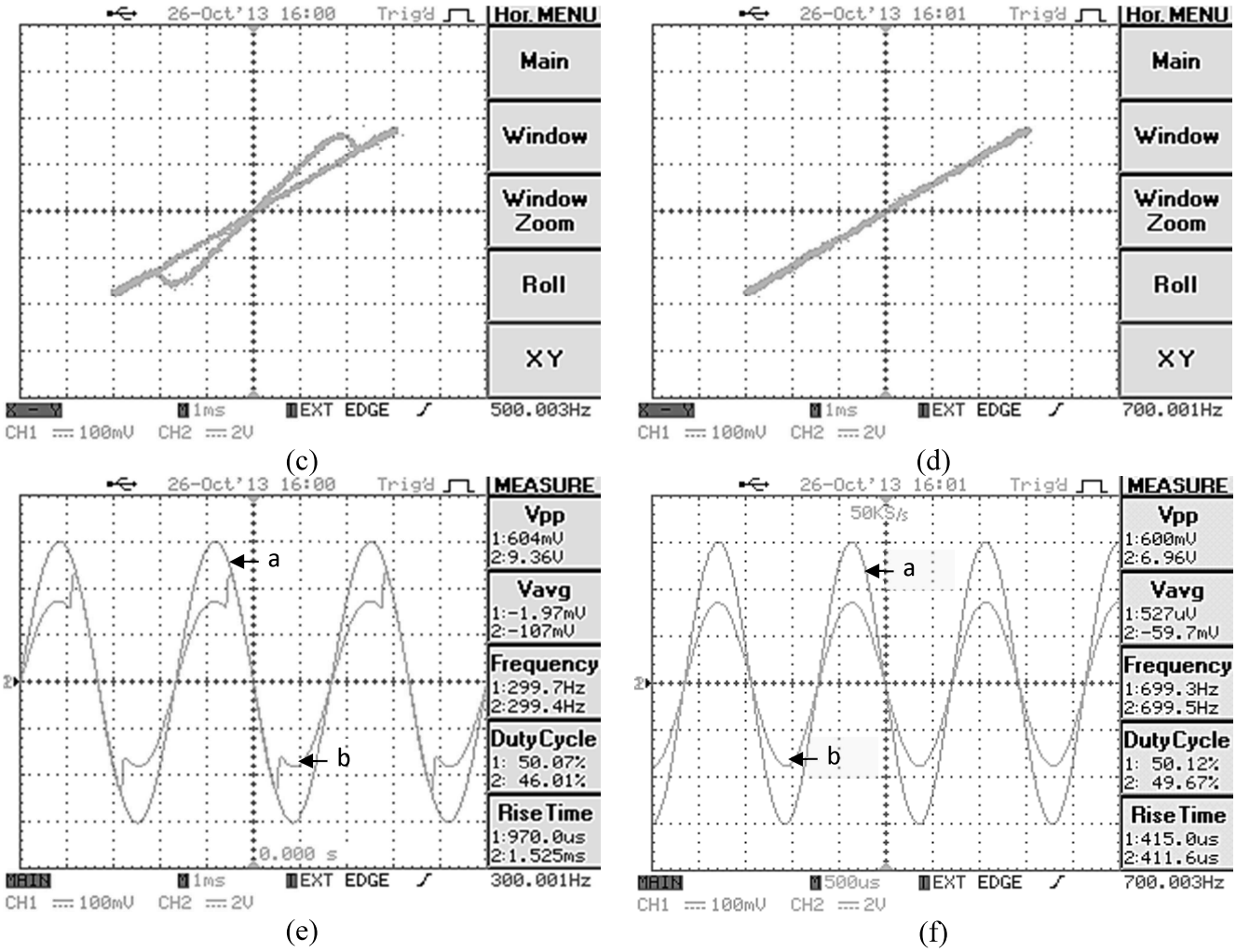



Figure 23: Characteristics of the low input impedance Mutator. (a) The v-i response at 100Hz. (b) The v-i response at 300Hz. (c) The v-i response at 500Hz. (d) The v-i response at 700Hz. (e) The current injected a and the voltage sensed b vs. time at 300Hz. (f) The current injected a and the voltage sensed b vs. time at 700Hz

## 2.2. Floating memristor circuit emulator

Having a floating memristor emulator is very useful in some applications. Applications such as the sinusoidal oscillator shown in Figure 17 where the memristor is replacing the resistances in the circuit. A proposed circuit for the floating-memristor mutator has been implemented and tested. The proposed circuit is shown in Figure 24. The circuit uses four CFOA, four capacitors, two diodes and five resistors at least. The circuit operates in the same way as the grounded emulator of Figure 21 operates by

mirroring the upper half to the lower half in the circuit. It acts as a floating emulator for the memristor. The capacitors are shunted with a 47 KΩ resistors. The values of the components used in the implementation are indicated in the schematics of Figure 24.

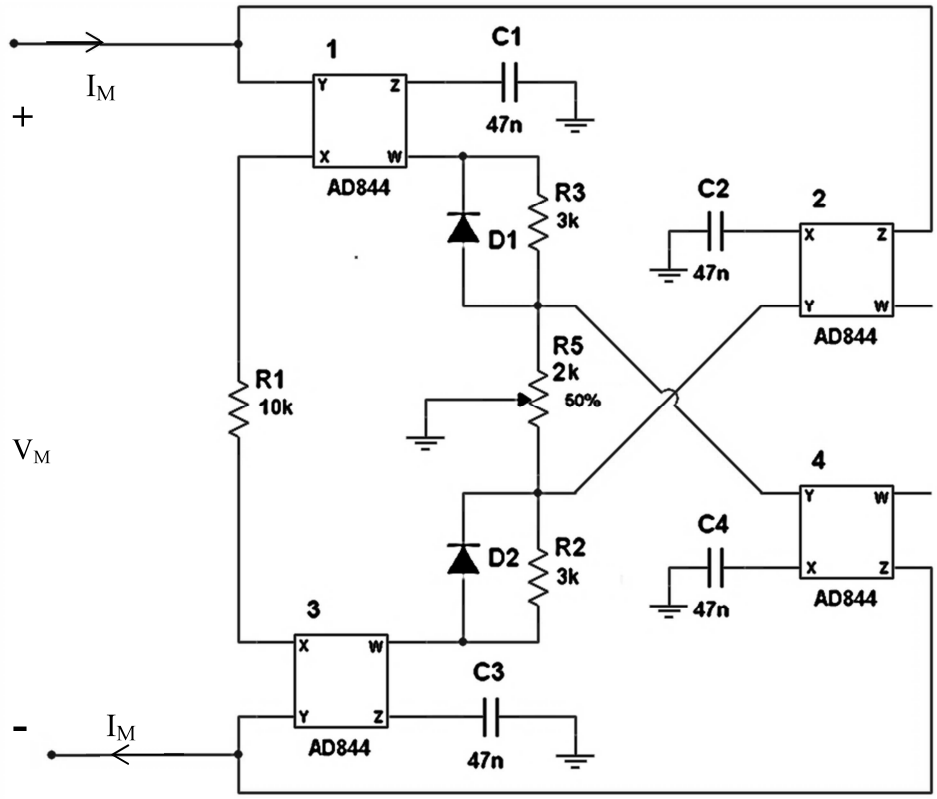
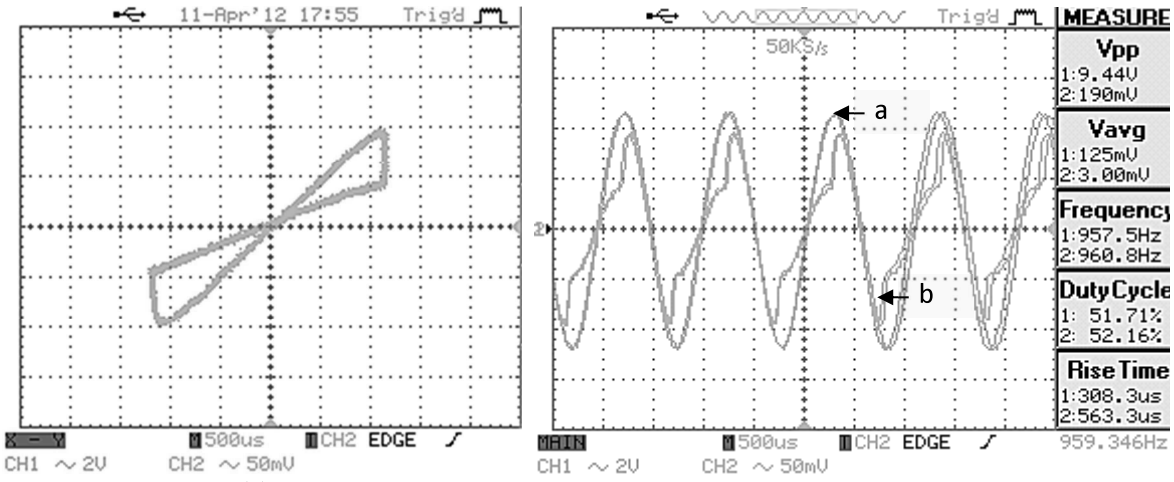



Figure 24: Proposed circuit for a floating-memristor mutator.

The circuit behavior, as illustrated in Figure 25 (a) and (b), shows that the circuit of Figure 24 emulates a memristor. The result shown is for an input signal at around 1 KHz. The circuit uses the concept of utilizing a non-linear resistor to have the bow-tie v-i curve. The circuit offers control over the values of $R_{LOW}$ and $R_{HIGH}$. The pairs (C1, C2), (C3, C4), (R2, R3) must be identical to have the same current in both terminals of the floating circuit. The same for the variable resistance, the voltage drop in one half must be

equal to the other half. The variable resistance is placed to have tunability to equalize the current in both terminals.




(a) (b)

Figure 25: (a) v-i curve of the floating-memristor mutator. (b) Voltage a and current b vs. time

A simple circuit showing the use of the floating memristor emulator is shown in Figure 26 for an OPAMP-based inverting amplifier. The floating memristor will replace one of the resistors and thus it will affect the current flowing through it. The input voltage-output voltage characteristic of the inverting amplifier will be as an inverted v-i curve of the memristor as shown in Figure 27. The values of $R_{LOW}$ and $R_{HIGH}$ can be estimated from the characteristics as around 10 KΩ and 2.5 KΩ respectively. The inverting amplifier gain is given in equation (3.11).

$$Gain = -\frac{R_a}{R_M} \tag{3.11}$$

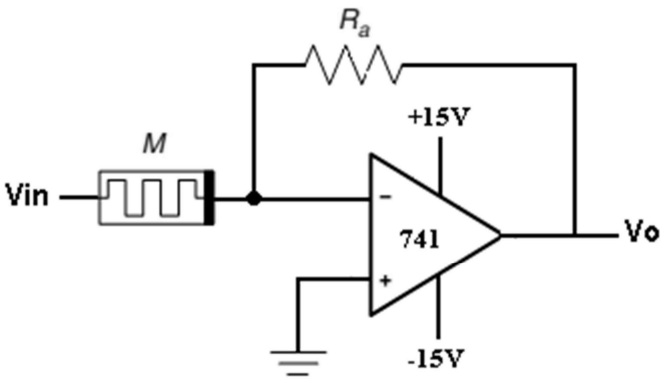



Figure 26: An implementation of the floating memristor using the proposed mutator. Where $R_a$ = 10 kΩ.

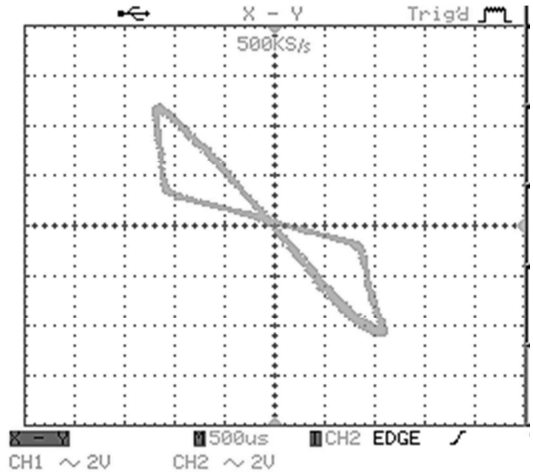



Figure 27: Vo vs. Vin of a simple inverting amplifier using the Memristor (Ra = 10 kΩ)

## 2.3. Discrete multi-state levels circuit emulator

The previous emulators offer binary state levels which mean that there are only two values of memristances. This is a disadvantage when an application such as an analog amplitude shift keying needs many amplitude levels to produce. The circuit in Figure 28 shows a circuit emulator that can have three states of memristance. As the voltage increases at terminal X of CFOA2, the diodes will turn forward and reduce the parallel resistance. This will change the gain of the non-linear scalar used here. The non-linear scalar has a positive gain which makes the memristor as a whole negative. An inverting buffer after the scalar can revert the polarity. The state levels can be controlled

using pulses at the input which will accumulate by the integrator to raise the voltage and thus changing the state level. The circuit is of type 2 realization 1 from the categorization in Table 1. By following the same approach in Figure 21, this circuit can be transformed to type 1 realization 1 as well.

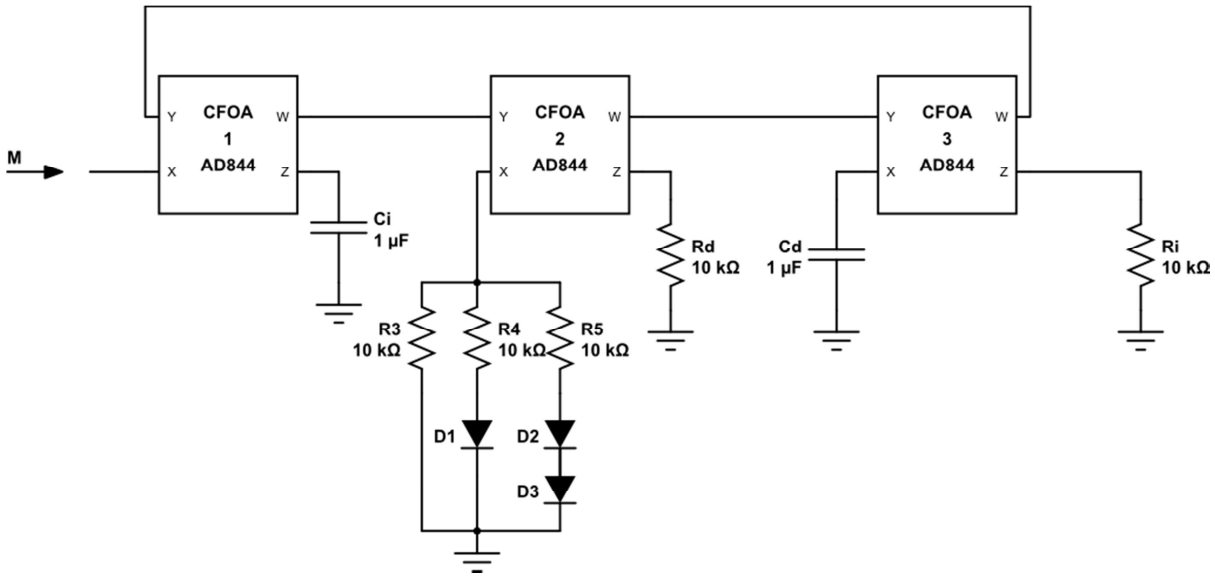



Figure 28: Discrete multi-state level circuit emulator (*with negative memristance)

The characteristics equations for the emulator are given in equation (3.12) and (3.13). Equation (3.14) shows the overall memristance. The memristance will have three values depending on the value of $R_{eq}$ which depend on the diodes states.

$$V_R = \frac{-1}{C_i}\int I_M dt \tag{3.12}$$

$$V_M = \frac{R_i R_d C_d}{R_{eq}}\frac{d}{dt}\, V_R \tag{3.13}$$

Dividing $V_M$ by $I_M$ from equation (3.12) and (3.13),

$$M = \frac{-R_d R_i C_d}{R_{eq} C_i} \tag{3.14}$$

where $R_{eq} = \begin{bmatrix} R_3 & ,if\ all\ diodes\ are\ off \\ R_3//R_4 & ,if\ diode\ D1\ is\ on\ only \\ R_3//R_4//R_5 & ,if\ all\ diodes\ are\ on \end{bmatrix}$

## 2.4. Continuous state level circuit emulator

In analog applications, the need for continuous levels for the memristor is important. Such applications include the memristor in oscillators or multivibrator as will be discussed later in chapter 3 of this thesis. The proposed circuit, shown in Figure 29, offers a slower transition between $R_{LOW}$ and $R_{HIGH}$ which gives it the continuity in the levels such that it can be swept for more levels. This was achieved using the non-linear characteristics of the operational transconductance amplifier (OTA) as the non-linear scalar shown in Figure 31(a). The memristance is described in equation (3.15). This emulator has been tested and used in the multivibrating oscillator successfully since the binary emulator is not suitable. The characteristics of this emulator are shown in Figure 30. Figure 30 (a) shows the waveforms obtained for the current through and the voltage across the memristor. Figure 30 (b) shows the v-i characteristics of Figure 29 by injecting a current and sensing the voltage across the memristor.

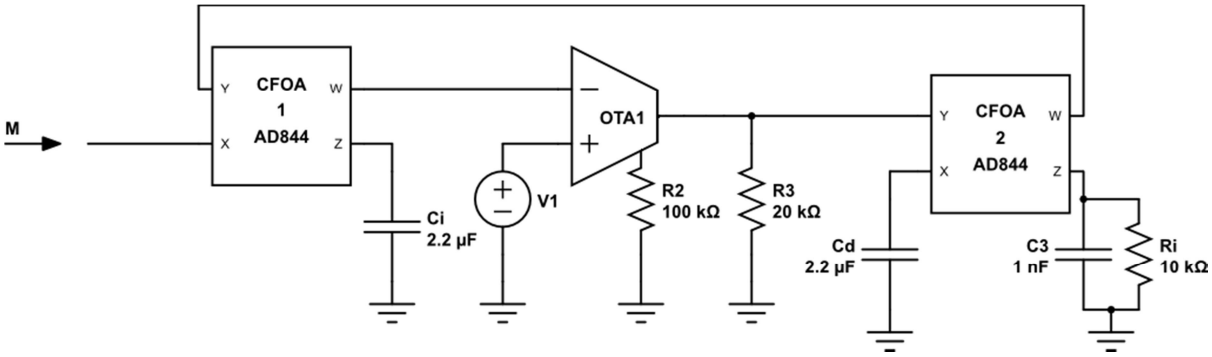
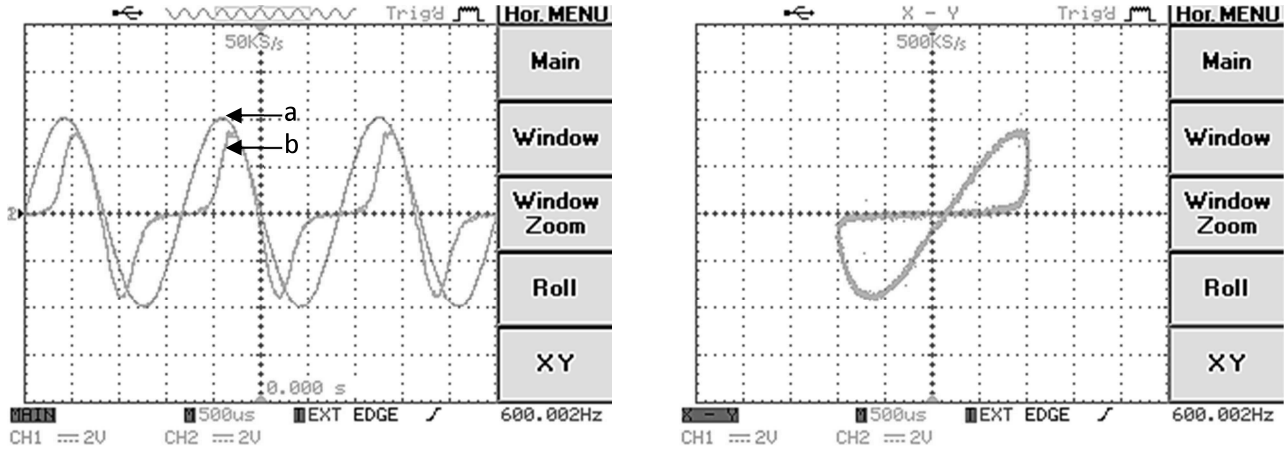



Figure 29: continuous state level circuit emulator

$$M = \frac{R_i C_d}{C_i} F \tag{3.15}$$

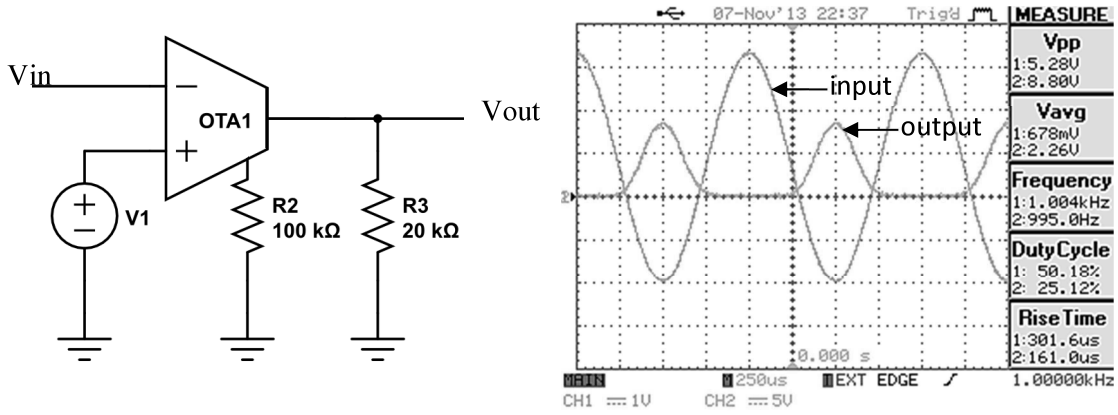
where F is the transfer function of the OTA circuit shown in Figure 32.




(a) (b)

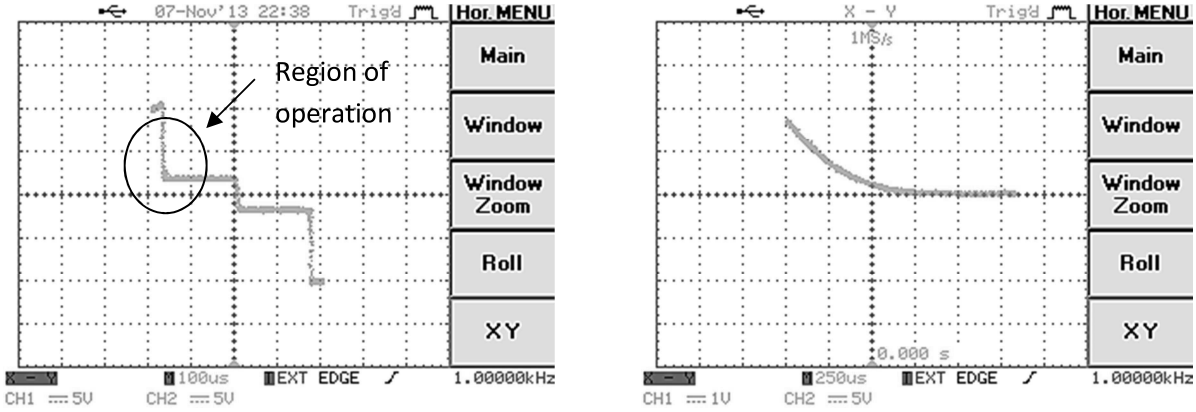
Figure 30: (a) The applied current a and the voltage across the memristor b vs. time (b) The v-i characteristic curve of the continuous level emulator

The non-linear scalar shown in Figure 31(a) is built using an OTA, two resistors and a DC voltage source. The resistor R2 will decide the bias current $I_{ABC}$ of the OTA. The output current of the OTA will induce a voltage across the resistor R3. The DC voltage source will determine the region of operation or in another word; it will bias the OTA to operate in the highly non-linear region shown in Figure 32. The response of the circuit shown in Figure 31(a) has been investigated. Figure 31(b) shows the output voltage when applying a voltage at the negative terminal of the OTA. It is clear that the positive half of the input signal is treated differently than the negative half and that the circuit as a whole has inverting characteristics needed to have the correct response for the memristance. The characteristics of the OTA shown in Figure 32 were obtained by applying a voltage at the negative terminal and having the positive terminal to ground. Using the DC voltage V1 at the positive terminal, the region of operation is selected as shown in Figure 32. V1 was set to 11.7V since the non-linearity at that region has much more dynamic range than the region around V1=0.




(a) (b)

Figure 31: (a) The non-linear scalar used in the continuous level memristor emulator. (b) Vin and Vout vs. time of testing the circuit in (a)




(a) (b)

Figure 32: (a) The transfer characteristic of the circuit in Figure 31(a) Vout vs. Vin by applying Vin = 20Vp-p.(b) The characteristic Vout vs. Vin at the region of interest by applying Vin = 5Vp-p and V1 = 11.7VDC.

## 2.5. Incremental and decremental circuit emulator

The polarity of the memristor indicates that for which direction of current flow, the memristance will decrease or increase. For the incremental type, as the voltage applied increases for a fixed amount of time, the resistance will increase while for the decremental type the resistance will decrease. This is applicable for the voltage driven memristor emulators but the same goes for the current driven type with current. Also, as

the time period of the pulse applied increases with a fixed amplitude, the resistance will increase for the incremental type and decrease for the decremental type. This is very important when the application depends on the increase or decrease of the memristance. Changing the polarity was achieved by controlling the non-linear circuit. Different polarities for the memristor emulator are shown in Figure 33 for voltage driven emulators and Figure 34 for current driven emulators. Using the proposed emulators, it is possible to change the polarity by just reversing the direction of the diode in the circuit. Referring to Figure 33 and Figure 34, the first circuit acts as an incremental memristor while the second circuit is the decremental one. The symbols are shown in the figures as well. In both circuits, as the integral of the applied signal over time, or the area under the curve of the voltage as a function of time v(t) or the current as a function of time i(t), increases, the diode will turn on or off thus the resistance will either increase or decrease.

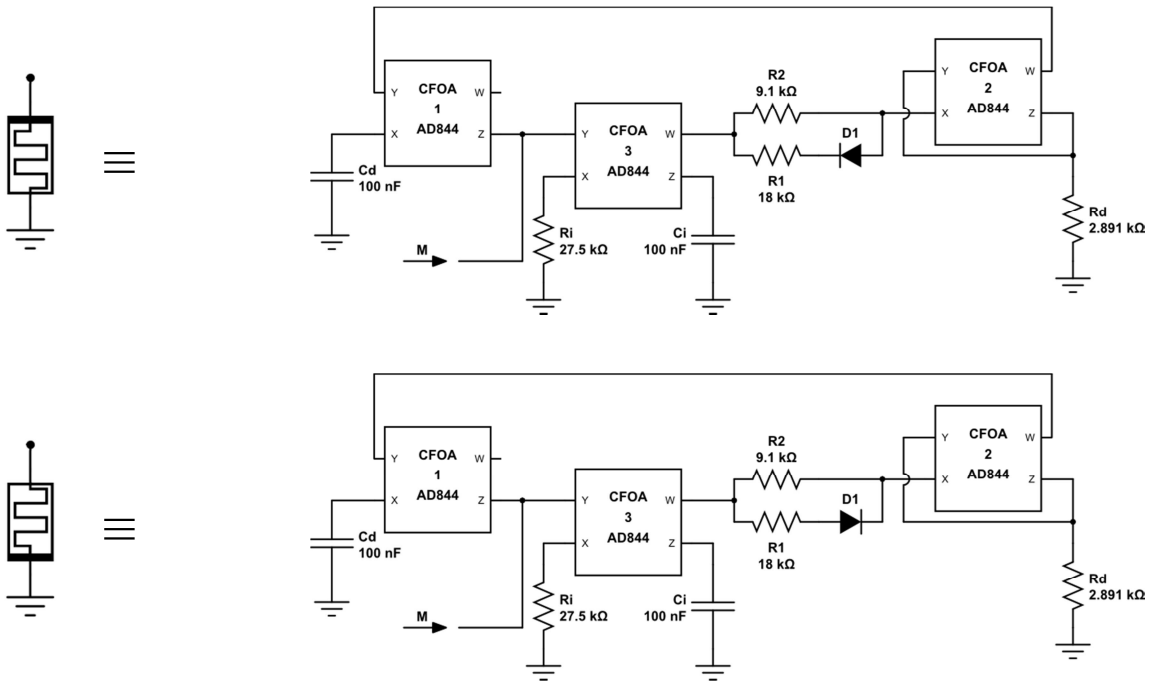



Figure 33: voltage driven memristor circuit emulator with different polarities, (Top) is the incremental type, (bottom) is the decremental type.

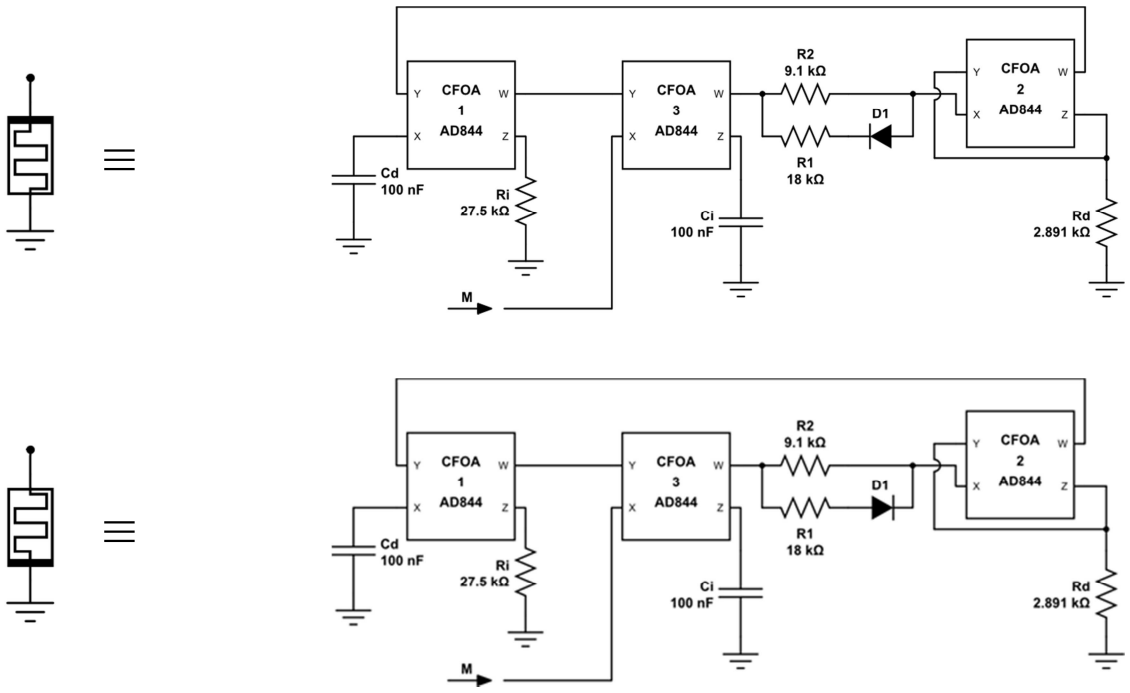



Figure 34: Current driven memristor circuit emulator with differnet polarities, (Top) incremental type, (Bottom) decremental type

Test results were obtained by applying a square wave to a series combination of a resistor and a grounded memristor as shown in Figure 35. Figure 35 shows the reaction of the output voltage whether it will increase or decrease depending on the polarity of the memristor. The transition position depends on the amplitude of the input signal and characteristics of the integrator in the emulator.

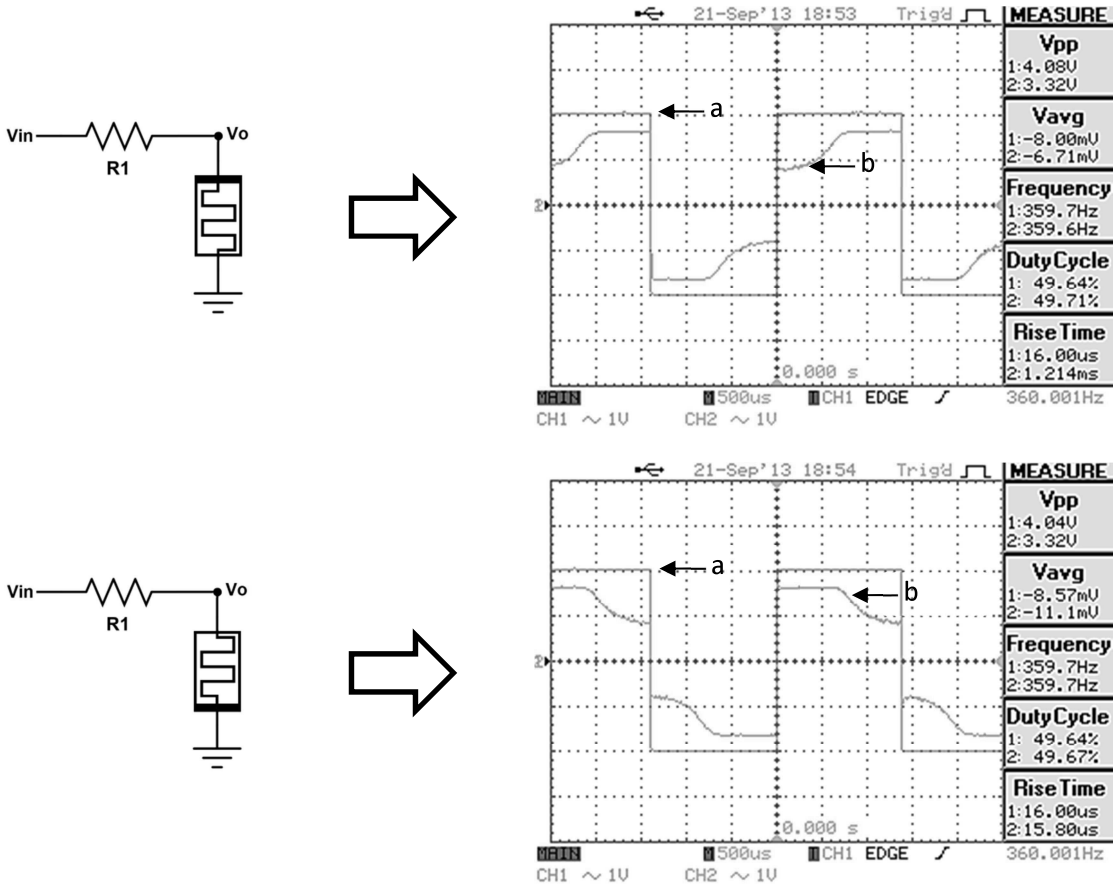



Figure 35: Test results by applying a square wave to different polarities of the memristor where a is the input voltage and b is the output voltage vs. time.

## 2.6. Negative memristor circuit emulator

The circuit, shown in Figure 36, operates as a negative memristor which means that it is no longer following the definition of the memristor but it is like a negative resistor. The voltage and current will have a 180 degree phase shift. The characteristics equations for the emulator are given in equation (3.16) and (3.17). Equation (3.18) shows the overall memristance that the circuit will have. The memristance will have two values depending on the value of $R_{eq}$ which depend on the diode state.

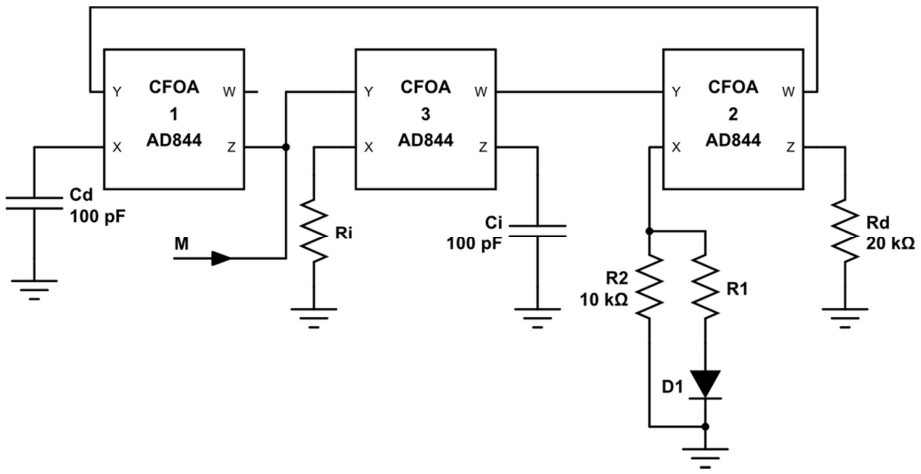



Figure 36: Negative memristor circuit emulator

$$V_R = \frac{-1}{C_i}\int I_M dt \tag{3.16}$$

$$V_M = \frac{R_i R_d C_d}{R_{eq}}\frac{d}{dt}\, V_R \tag{3.17}$$

Dividing $V_M$ by $I_M$ from equation (3.16) and (3.17),

$$M = \frac{-R_d R_i C_d}{R_{eq} C_i} \tag{3.18}$$

where $R_{eq} = \begin{bmatrix} R_3 & ,if\ the\ diodes\ are\ off \\ R_3 // R_4 & ,if\ the\ diode\ is\ on \end{bmatrix}$

# Chapter 3

# Implemented Applications

## 3.1. Memristor Based Multivibrating Oscillator

Using the memristor in multi-vibrating oscillator is very attractive since the memristor will replace the capacitor giving us a reactance-less oscillator. The circuit in Figure 37 shows an oscillator circuit proposed in [18]. This circuit can then be modified to achieve a voltage controlled oscillator as proposed in [19] by applying a voltage reference instead of the ground in the terminal of the memristor. These circuits have been implemented using the circuit shown in Figure 38 and Figure 39 utilizing the continuous-nonlinear levels of the circuit emulator shown in Figure 29. In [18] and [19], a simulation was carried out using the ideal emulator of the memristor. However, in this work, hardware results were obtained using the circuit emulator.

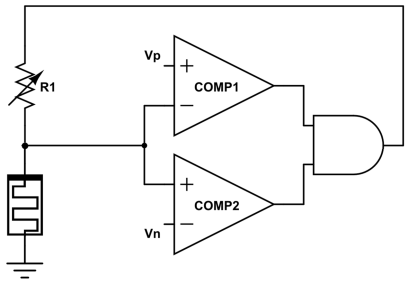



Figure 37: Multi-vibrating Oscillator proposed by [18]

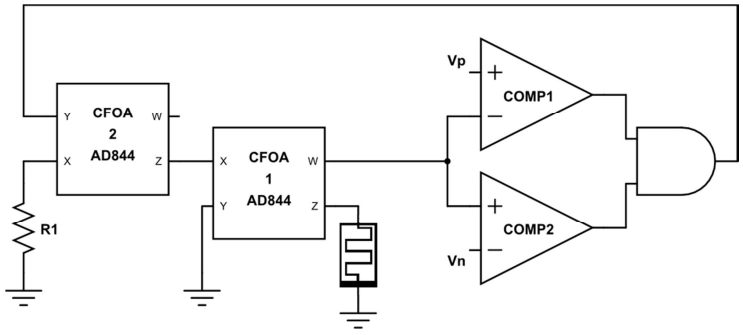



Figure 38: Implemented circuit for a memristor based multi-vibrating oscillator

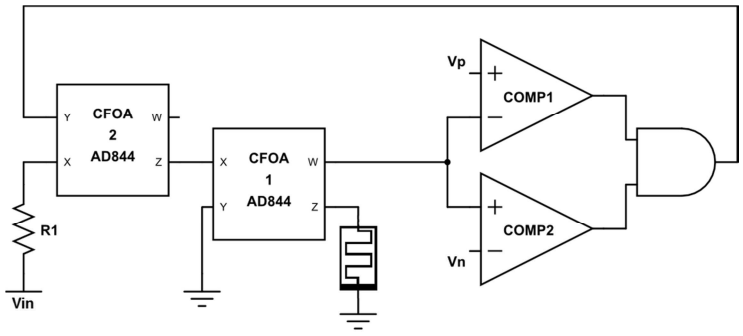



Figure 39: Implemented circuit for a memristor based multi-vibrating voltage-controlled oscillator

The circuit operates by allowing a certain flow of current through the memristor which will change the state level and thus change the resistance. If the memristor polarity is incremental as in Figure 37, the memristacnce will increase as the current flows through it. Increasing the memristance will increase the voltage across the memristor. The comparators circuit and the AND gate will control the output based on the voltage across the memristor. The transfer function of the two comparators and the AND gate is illustrated in Figure 40. If the voltage is more than $V_p$ and less than $V_n$, the output will be VoL and if the voltage is between $V_p$ and $V_n$, the output will be VoH. So changing the resistance R1 and the constant voltages $V_p$ and $V_n$ will control the frequency.

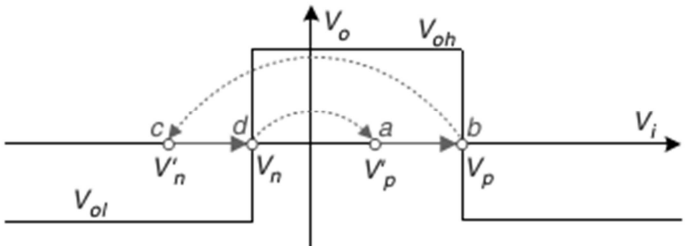



Figure 40: Transfer function of the comparator circuit [18]

Figure 41 shows the output wave form and the voltage across the memristor obtained by the implementation of Figure 38. Figure 42 shows the simulated results as reported in [18]. The dashed lines indicate the levels of $V_p$ and $V_n$. The response is different from [18] and [19] since it does not follow the ideal model but a non-linear model. The non-linearity in the emulator comes from the non-linear scalar used. This difference is shown clearly in the results of Figure 41 and Figure 42 of the voltage across the memristor waveform.

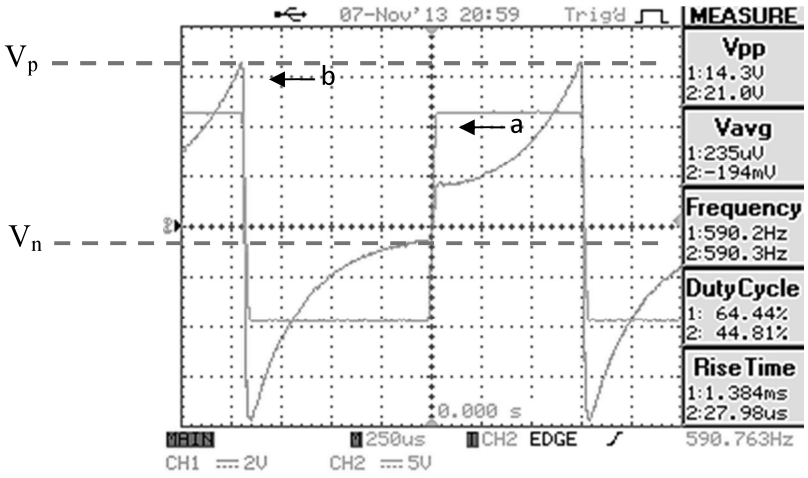



Figure 41: The Output wave form for the multi-vibrating oscillator
(a: output, b: the voltage across the memristor vs. time)

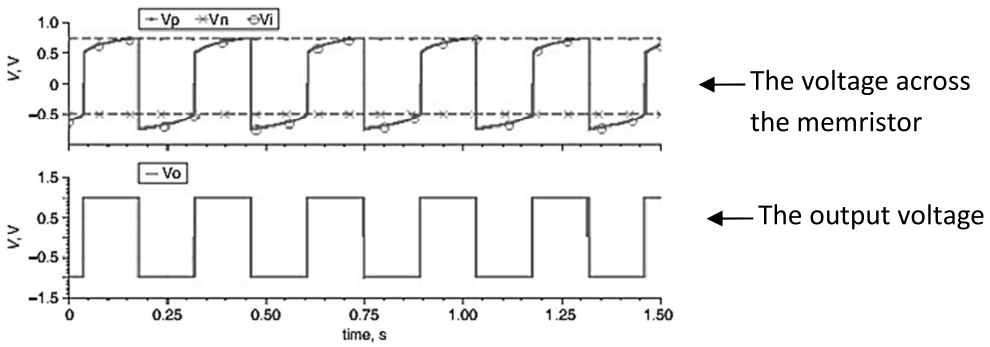



Figure 42: Simulation results as reported in [18]

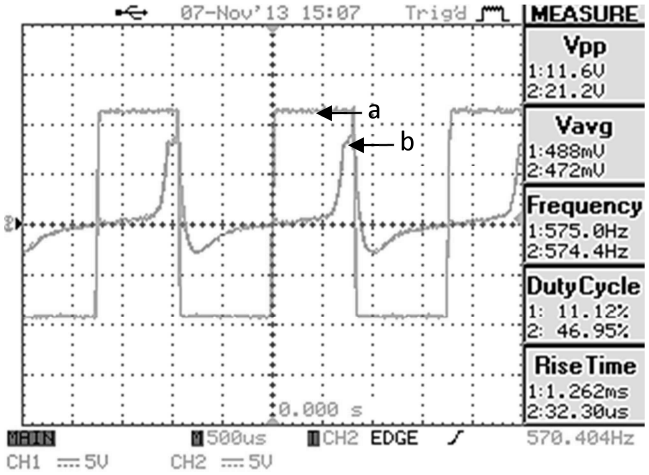
Table 3 shows different results of implementing Figure 38 with changing the parameters R1 while the other values are constant then changing $V_p$ and then with changing $V_n$. The value of Ri in the emulator of Figure 29 was set to 60 kΩ. Table 4 shows different results of implementing Figure 38 with changing the values of $V_p$ and $V_n$ and fixing the value of R1. The value of Ri in the emulator of Figure 29 for this case was set to 3.5 kΩ. Different frequencies were acquired by changing these parameters. Figure 43 shows different selected samples of the output voltage and the voltage across the memristor. The letters in the last column of Table 3 and Table 4 points to the different results and plots in Figure 43. From the figures, the non-linearity of the emulator is affecting the duty cycle as well as the frequency.

Table 3: Results of implementing Figure 38 with changing R1 while other values are constant then changing $V_p$ and the last part is with changing $V_n$ with Ri (Figure 29) = 60 kΩ, DC supply is V+ = 12V and V- = -12V

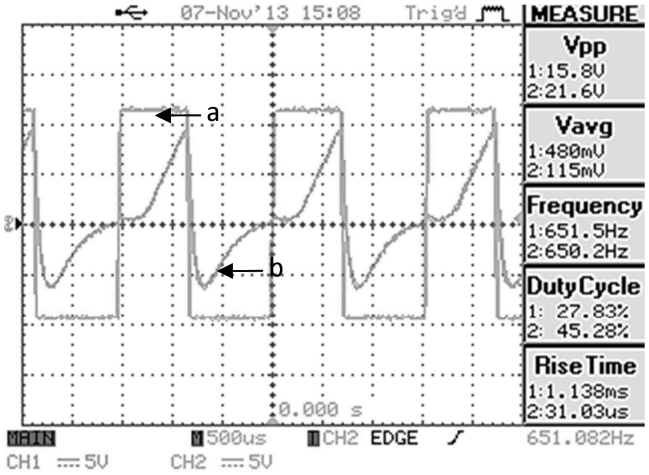
| R1 | freq | Duty Cycle% | Vp | Vn | Sample selected for Figure 43 |
|---|---|---|---|---|---|
| 1k | 489 | 45.2 | 7.8 | -0.73 | |
| 1.5k | 570 | 47 | 7.8 | -0.73 | a |
| 2k | 664 | 47.1 | 7.8 | -0.73 | |
| 3k | 791 | 46.3 | 7.8 | -0.73 | |
| 4.3k | 651 | 45.3 | 7.8 | -0.73 | b |
| 5.6k | 578 | 44.8 | 7.8 | -0.73 | c |
| 6.8k | 427 | 57 | 7.8 | -0.73 | |
| 10k | 309 | 65 | 7.8 | -0.73 | d |
| 15k | 213 | 72 | 7.8 | -0.73 | |
| 47k | 73.8 | 86 | 7.8 | -0.73 | e |
| 5.6k | 1121 | 45 | 1.55 | -0.73 | |
| 5.6k | 897 | 45 | 2.0 | -0.73 | f |
| 5.6k | 818 | 45 | 2.5 | -0.73 | |
| 5.6k | 591 | 45 | 5.2 | -0.73 | |
| 5.6k | 1530 | 44 | 2.5 | -1.4 | g |
| 5.6k | 1993 | 44 | 2.5 | -1.8 | |

Table 4: Results of implementing Figure 37 with changing $V_p$ and $V_n$ with Ri (Figure 29) = 3.5 kΩ

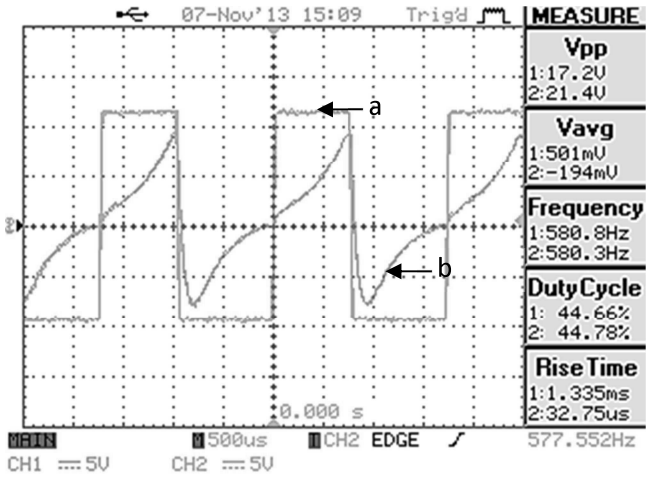
| R1 | freq | Duty Cycle% | Vp | Vn | Sample selected for Figure 43 |
|---|---|---|---|---|---|
| 5.6k | 1985 | 45 | 2.4 | -1.57 | h |
| 5.6k | 1233 | 45.3 | 3.4 | -1.57 | i |
| 5.6k | 379 | 45 | 2.4 | -0.27 | |
| 5.6k | 3780 | 44.3 | 3.3 | -2.76 | j |



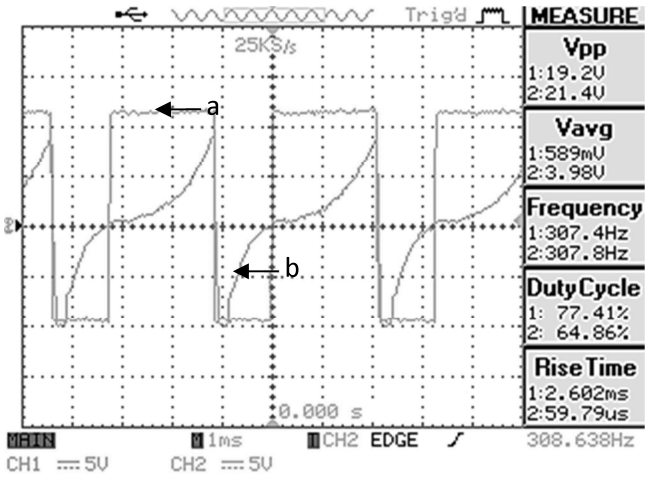

(a)



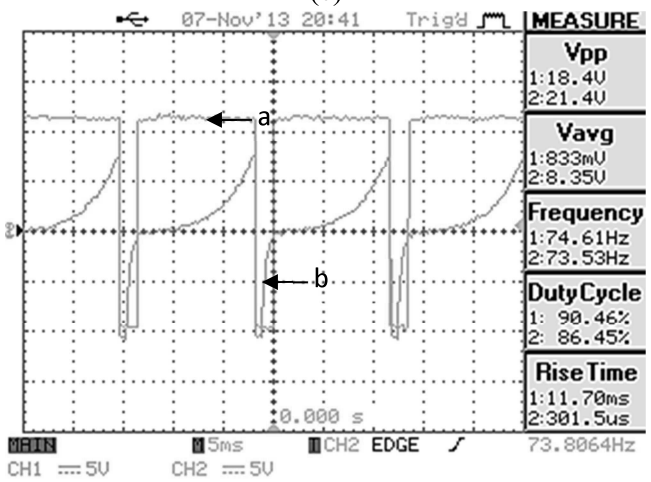

(b)


07-Nov'13 15:09
Trig'd
MEASURE
Vpp
1:17.2V
2:21.4V
Vavg
1:501mV
2:-194mV
Frequency
1:580.8Hz
2:580.3Hz
Duty Cycle
1: 44.66%
2: 44.78%
Rise Time
1:1.335ms
2:32.75us
a
b
0.000 s
MAIN
500us
CH2 EDGE
577.552Hz
CH1 5V
CH2 5V

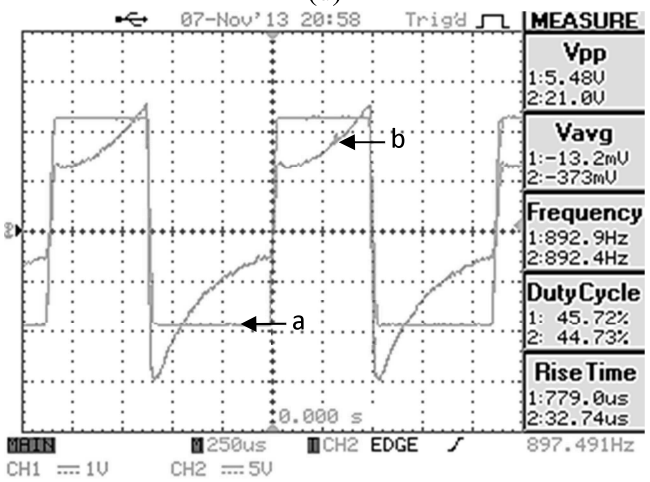
(c)


Trig'd
25KS/s
MEASURE
Vpp
1:19.2V
2:21.4V
Vavg
1:589mV
2:3.98V
Frequency
1:307.4Hz
2:307.8Hz
Duty Cycle
1: 77.41%
2: 64.86%
Rise Time
1:2.602ms
2:59.79us
a
b
0.000 s
MAIN
1ms
CH2 EDGE
308.638Hz
CH1 5V
CH2 5V

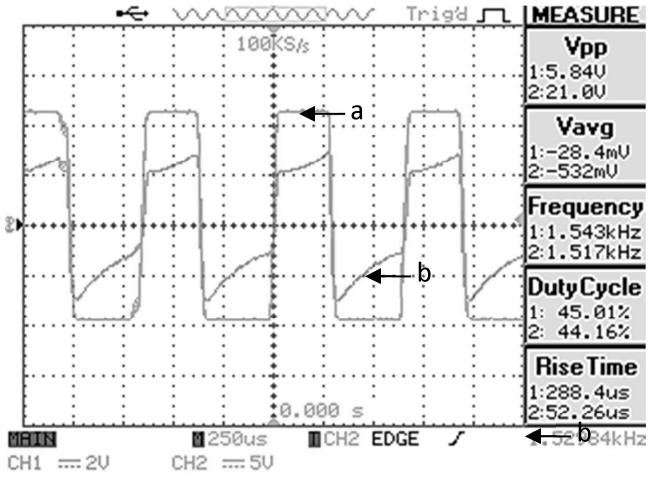
(d)


07-Nov'13 20:41
Trig'd
MEASURE
Vpp
1:18.4V
2:21.4V
Vavg
1:833mV
2:8.35V
Frequency
1:74.61Hz
2:73.53Hz
Duty Cycle
1: 90.46%
2: 86.45%
Rise Time
1:11.70ms
2:301.5us
a
b
0.000 s
MAIN
5ms
CH2 EDGE
73.8064Hz
CH1 5V
CH2 5V

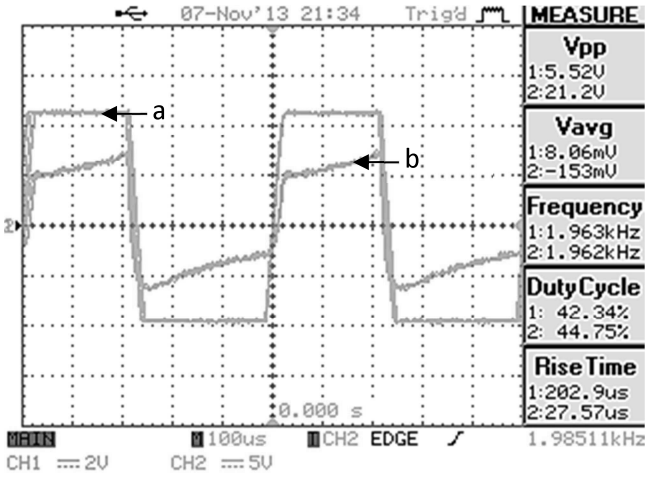
(e)


07-Nov'13 20:58
Trig'd
MEASURE
Vpp
1:5.48V
2:21.0V
Vavg
1:-13.2mV
2:-373mV
Frequency
1:892.9Hz
2:892.4Hz
Duty Cycle
1: 45.72%
2: 44.73%
Rise Time
1:779.0us
2:32.74us
b
a
0.000 s
MAIN
250us
CH2 EDGE
897.491Hz
CH1 1V
CH2 5V

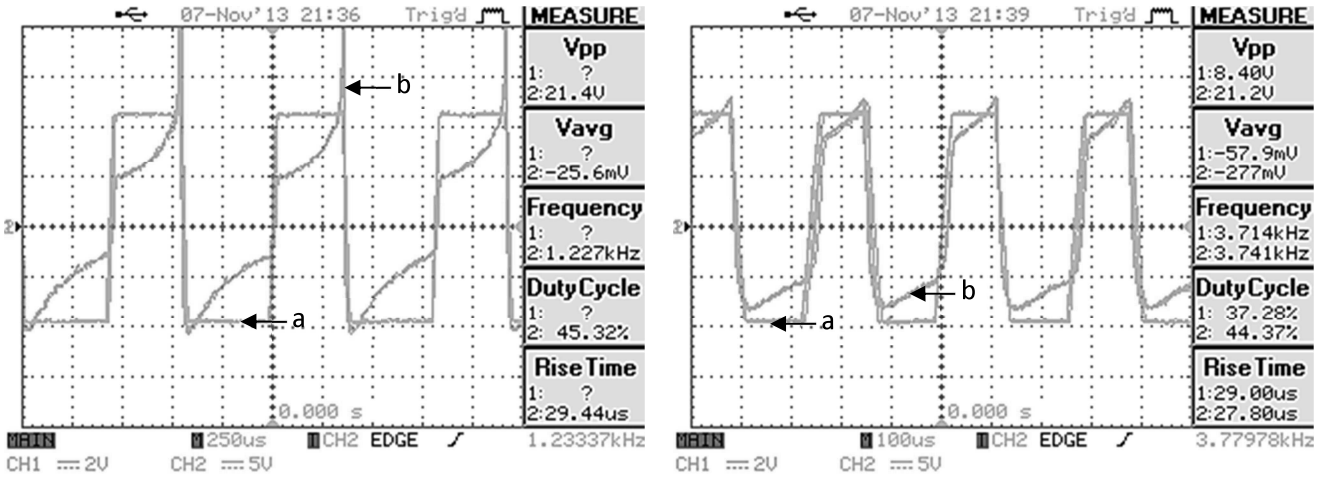
(f)


Trig'd
100KS/s
MEASURE
Vpp
1:5.84V
2:21.0V
Vavg
1:-28.4mV
2:-532mV
Frequency
1:1.543kHz
2:1.517kHz
Duty Cycle
1: 45.01%
2: 44.16%
Rise Time
1:288.4us
2:52.26us
a
b
0.000 s
MAIN
250us
CH2 EDGE
CH1 2V
CH2 5V

(g)


07-Nov'13 21:34
Trig'd
MEASURE
Vpp
1:5.52V
2:21.2V
Vavg
1:8.06mV
2:-153mV
Frequency
1:1.963kHz
2:1.962kHz
Duty Cycle
1: 42.34%
2: 44.75%
Rise Time
1:202.9us
2:27.57us
a
b
0.000 s
MAIN
100us
CH2 EDGE
1.98511kHz
CH1 2V
CH2 5V

(h)




(i) (j)

Figure 43: Different samples of output wave forms of implementing Figure 38 (a is the output and b is the voltage across the memristor vs. time), Details of each response is in Table 3 and Table 4

Using the circuit of Figure 39, applying a voltage to $V_{in}$ terminal will change the frequency and the duty cycle. The results in Figure 44 were obtained by implementing the circuit and changing the value of $V_{in}$. It operates as if the resistance R1 is changing when connected to ground thus controlling the current fed to the memristor. As the voltage increases, the current fed to the memristor will decrease. This will increase the time period where the memristance value will reach the threshold limits $V_p$ or $V_n$. Consequently the frequency will decrease as shown from the experimental results of Figure 44.

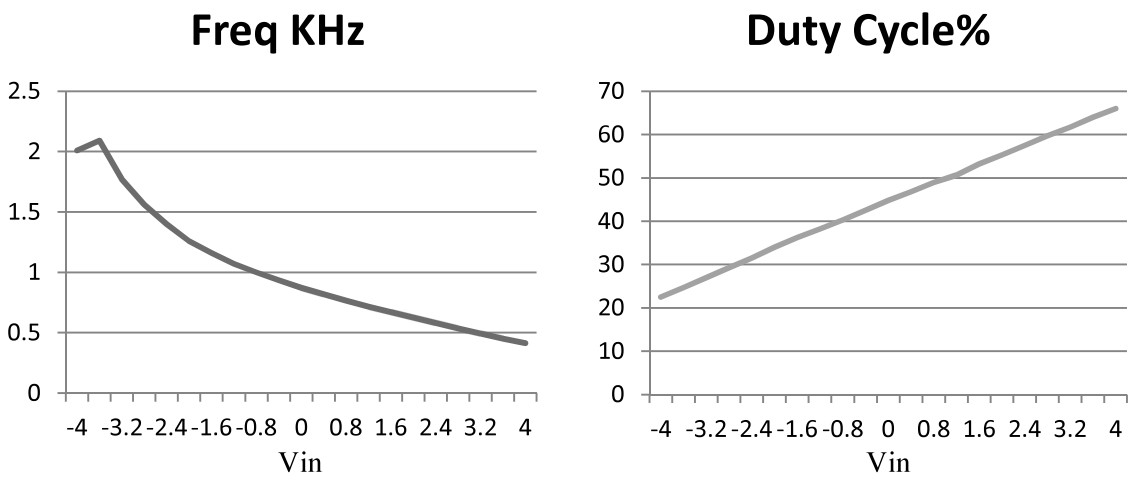



Figure 44: Results of implementing the voltage controlled multvibrator circuit shown in Figure 39

## 3.2. Memristor Based Signal Modulation Circuits

The controllable change in the resistance of the memristor, or the memristance, can be exploited in signal modulation and tunable filters. Signal modulation such as amplitude modulation, amplitude shift keying (ASK), ON-OFF keying, frequency shift keying (FSK) and binary phase shift keying (BPSK) has been proposed in several publications [21][22]. A tunable filter utilizing the memristor properties was proposed in [20].

The state level of the memristor can be changed, thus changing the memristance, by applying pulses. From equations (2.9) and (2.10), applying a relatively fast signal, relative to the mobility of the dopants, with zero DC components will barely change the state level of the memristor. However, if the signal applied is relatively slow, the state level will change between the limits ($R_{LOW}$-$R_{HIGH}$). Using this key behavior, applying an AC-high-frequency signal with zero DC-component will make the memristor to act as a normal resistance that can be controlled by applying pulses.

Using the circuit emulator proposed in Figure 22, several applications have been implemented including a programmable amplifier or an amplitude shift keying circuit, programmable differentiator, frequency shift keying circuit and a binary phase shift keying circuit. The memristor emulator used is the binary low impedance input type shown in Figure 45. The pulse applied to change the memristance will be integrated in CFOA3 and the resulted voltage will appear at terminal w. Depending on the value of the voltage, the diode will either be on or off thus controlling the gain in the non-linear scalar. Then the integrated signal is differentiated and fed back as a voltage across the memristor. A drawback of using this emulator appears in the integrator because of the non-ideality of the CFOA. The bias current will discharge the collected or integrated charge on the capacitor depending on the output resistance of the terminal Z. Approximately, the change will withhold for about a second then it will discharge enough to turn the diode off again. This can be calculated considering the output resistance is around 2MΩ and the capacitor is 101nF (time of discharge ≈ 5CR = 1sescond). A shunt resistor might be added in parallel with the integrator capacitance on terminal Z of CFOA3 to avoid saturation that is using a non-ideal integrator. This might reduce the time of discharge but it is a compromise that had to be taken.

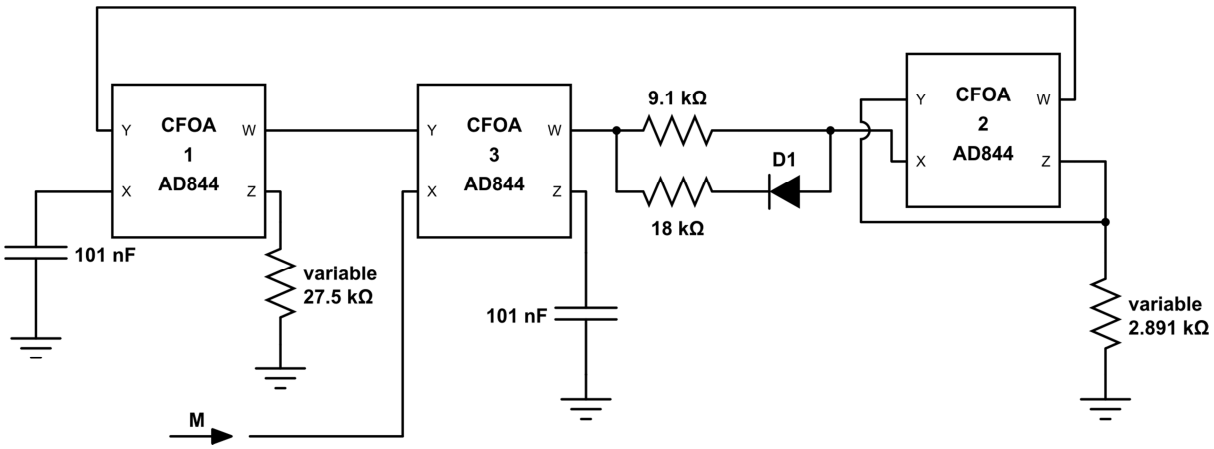



Figure 45: Memristor emulator used

### 3.2.1. Memristor Based ASK Modulation

The circuit shown in Figure 46 is a memristor-based voltage amplifier. Straight forward analysis leads to equation (4.1) describing the relationship between the input and the output voltage. According to equation (4.1), the gain is proportional to the memristance. The memristance can be controlled using the DC biasing current source $I_P$. The current pulses were supplied using the circuit in Figure 47. The pulses were generated using a 555 timer circuit in mono stable mode.

The gain in this case will have two values, one when the memristance is set to $R_{LOW}$ and one when the memristance is set to $R_{HIGH}$. The outputs are shown in Figure 48 for the output before applying the pulse and after applying the pulse.

Table 5 shows the gain and the memristance calculated from the two output states according to equation (4.1).

$$\frac{V_o}{Vi} = \frac{M}{R} \tag{4.1}$$

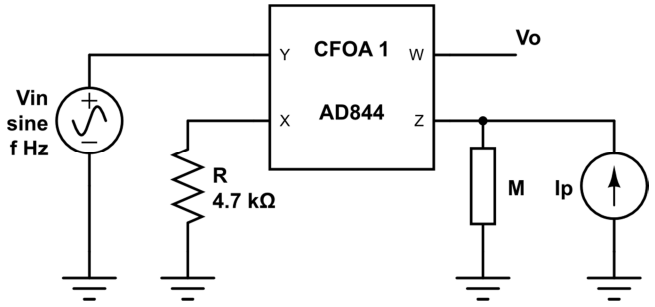



Figure 46: Amplifier using Memristor

Calculating the memristance of each state from the results with R = 4.7KΩ,

Table 5: Results of implementing the circuit in Figure 46

| $I_P$ (mA) | M (Ω) | Gain (Vo/Vin) |
|---|---|---|
| ≈0 | 14.1k | 6/2 |
| 3 | 24.6k | 10.5/2 |

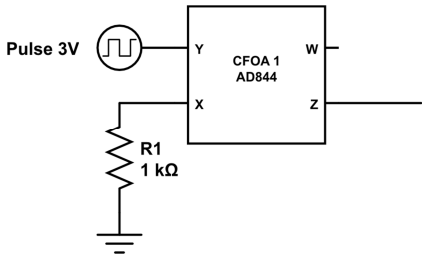
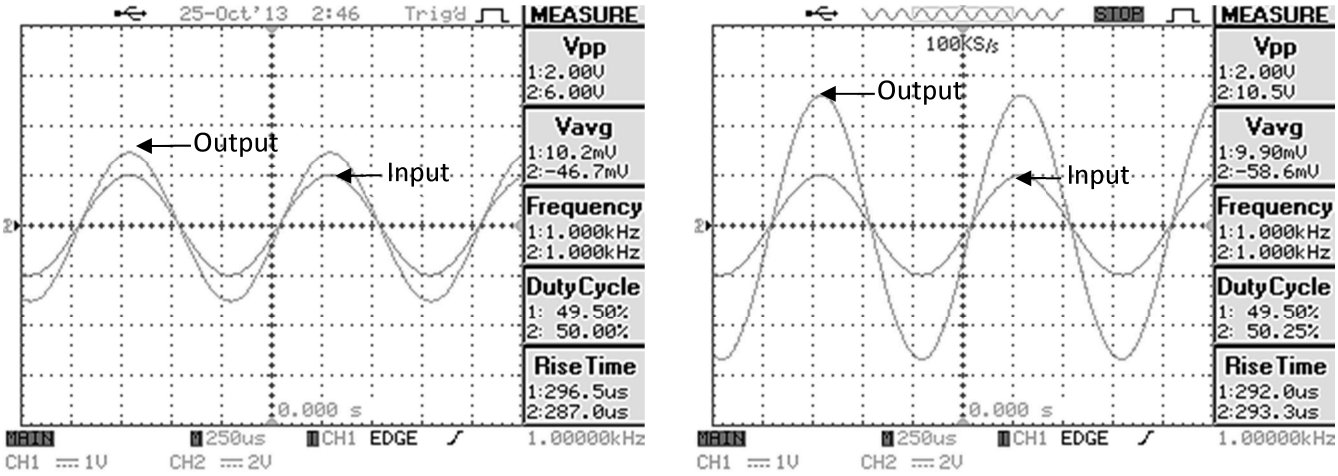



Figure 47: current pulses source circuit




(a) (b)

Figure 48: (a) Input and output signal after applying the pulse vs. time (b) Input and output signal before applying the pulse vs. time.

Figure 49 shows the variation of the output signal amplitude with an input binary sequence; that is $I_P$ has two values. The input can be a message from a digital circuit. Because the frequency of the binary signal is relatively close to the discharge time of the integrating capacitor, referring to Figure 45, a gradual change is occurring in the amplitude of the output signal. This will define the maximum frequency of the message signal.

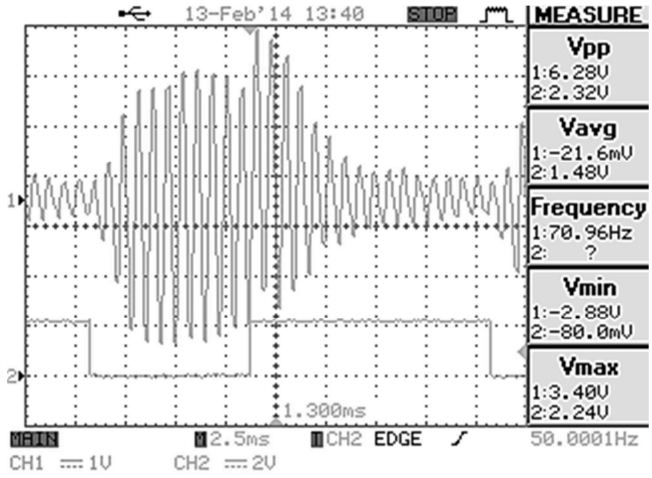



Figure 49: The output sinusoidal signal and a binary message input signal vs. time.

### 3.2.2. Memristor Based Tunable Differentiator

Figure 50 shows a programmable differentiator utilizing the memristor behavior. The outputs are shown in Figure 51 for different values of $I_P$. Straight forward analysis leads to equation (4.2) describing the relationship between the input and the output voltage.

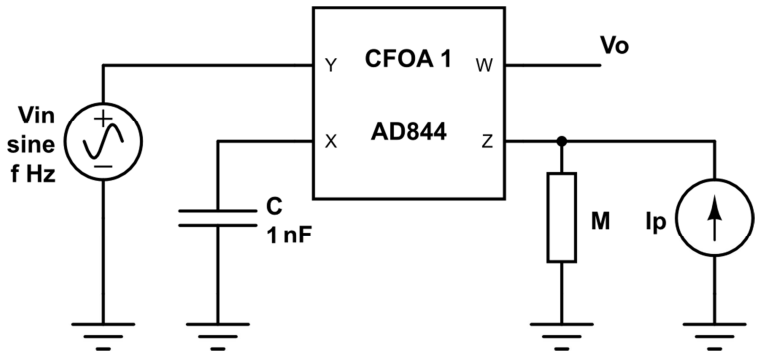


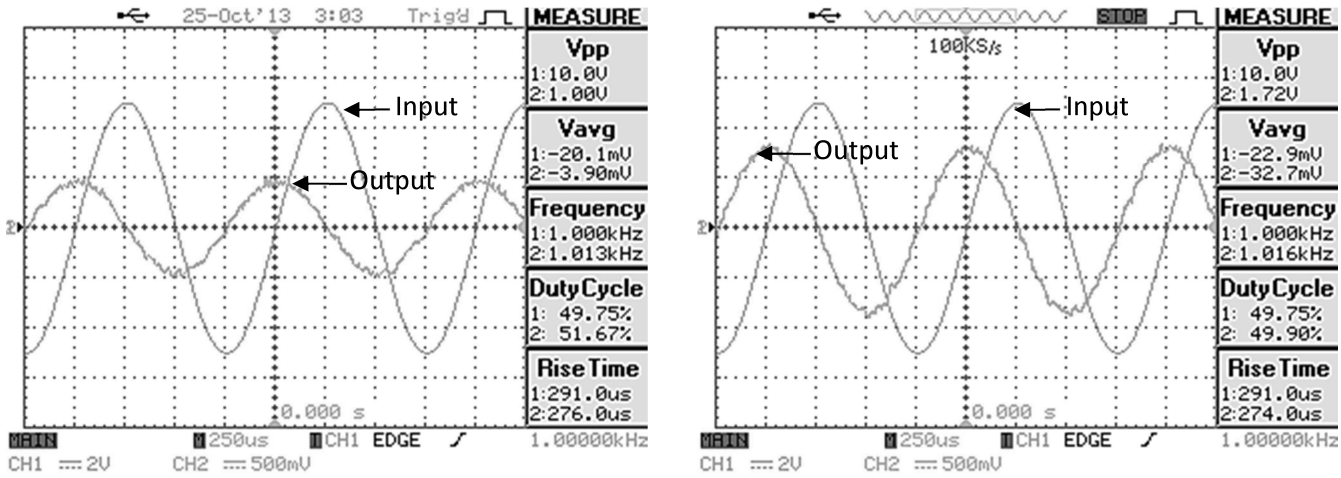

Figure 50: A differentiator circuit using Memristor

$$\frac{V_o}{V_i} = sCM \tag{4.2}$$

Using the results in Figure 51 and using equation (4.2), the memristance can be calculated, shown in Table 6.

Table 6: Results of implementing the circuit in Figure 50

| $I_P$ (mA) | G @ 1KHz | M(Ω) |
|---|---|---|
| ≈0 | 1/10 | 15.9k |
| 3 | 1.72/10 | 27.4k |




(a) (b)

Figure 51: input and output signal before applying the pulse vs. time (b) Input and output signal after applying the pulse vs. time.

### 3.2.3. Memristor Based FSK Modulation

The circuit shown in Figure 52 is a programmable oscillator utilizing the memristor. Straight forward analysis leads to the characteristic equation of this oscillator shown in equation (4.3). Figure 53, (a) and (b), shows the output waveforms before and after applying the tuning pulse giving two states for the memristor. The memristance, as shown in equation (4.3), will affect the frequency of oscillation thus the tuning pulse will tune the frequency of oscillation.

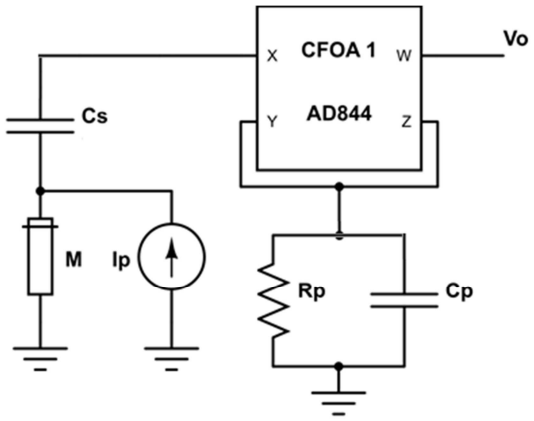



Figure 52: Circuit diagram for the memristor based FSK modulation

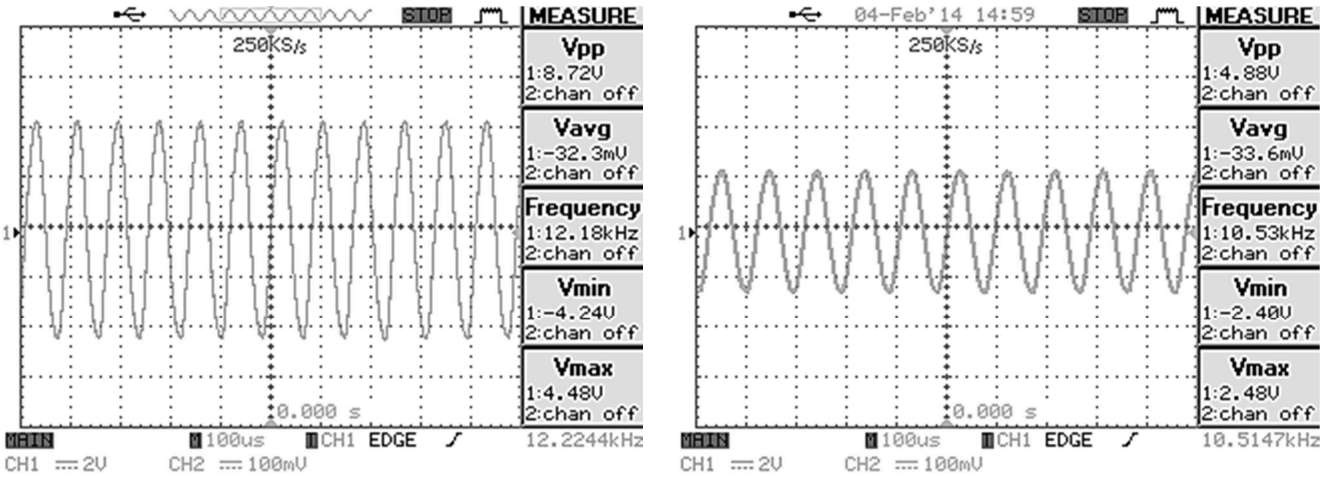
$$s^2 C_s C_p R_p M + s\left(C_p R_p + C_s M - C_s R_p\right) + 1 = 0 \tag{4.3}$$

From equation (4.3), the frequency and the condition of oscillator are given in equation (4.4) and (4.5).

$$w^2 = \frac{1}{C_s C_p R_p M} \tag{4.4}$$

$$C_s R_p \geq C_p R_p + C_s M \tag{4.5}$$

Where $C_s = 4.7nF, C_p = 3.3nF$ and$R_p = 25k\Omega$.




(a) (b)

Figure 53: (a) The output voltage vs. time before applying a pulse (b) The output voltage vs. time after applying the pulse

Figure 54 shows the variation of the output frequency with an input binary sequence. Because the frequency of the binary signal is relatively close to the discharge time of the integrating capacitor, referring to Figure 45, a gradual change is occurring in the frequency of the output signal. This will define the maximum frequency of the binary input signal.

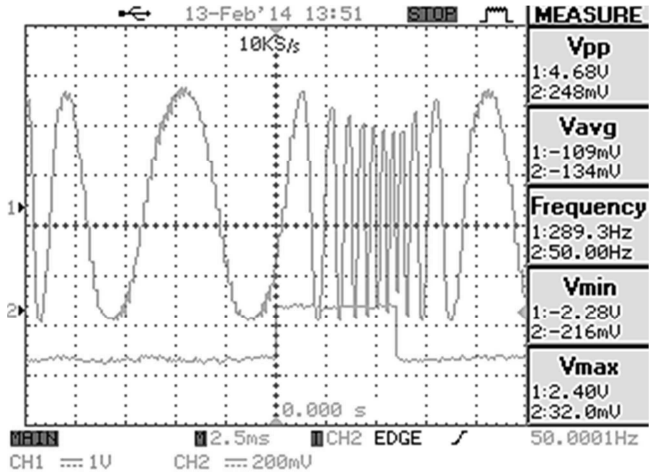



Figure 54: The output FSK modulated signal vs. time and a binary message input signal vs. time

### 3.2.4. Memristor Based BPSK Modulation

A binary phase shift keying was implemented based on the simulation work done in [21]. The topology of the system is shown in Figure 15. Based on that topology, the circuit in Figure 55 was developed.

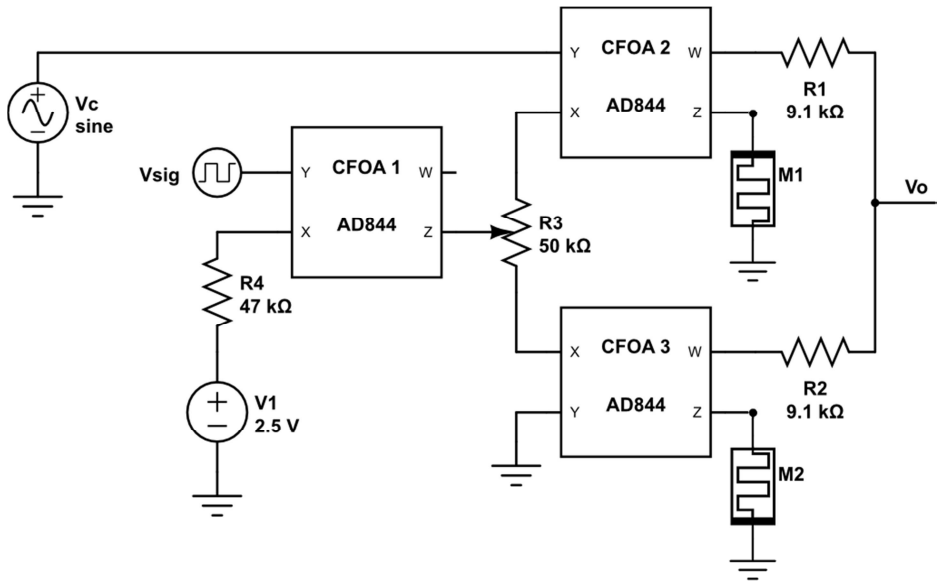
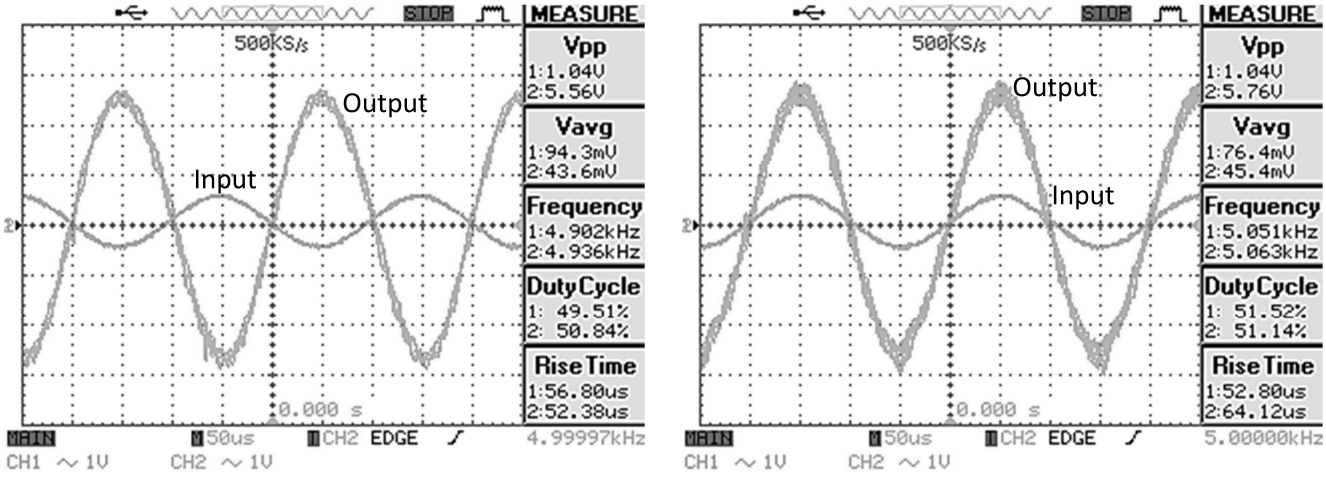



Figure 55: Circuit diagram for the memristor based BPSK modulation

Referring to Figure 55, the circuit should produce an output on a certain phase when the input voltage from Vsig is on one level and the output should be at 180 degree phase shift when Vsig is on the other level. Vsig will control the state of the memristors. If M1 is at $R_{LOW}$, M2 must be at $R_{HIGH}$ and vice versa. For an ideal situation, the values of $R_{LOW}$ and $R_{HIGH}$ should be for $R_{LOW}$ to be zero and $R_{HIGH}$ to be infinity but in reality it is preferred to have the ratio of $R_{HIGH}$ over $R_{LOW}$ to be as high as possible. This is so that the summation circuit, R1 and R2, produces a single phase at a time with minimum contribution from the opposite phase. Vc is the carrier signal running at around 12Vp-p. Vsig is a TTL digital signal with voltage levels zero and five volts. CFOA1 is a

preprocessing circuit to condition the input signal and convert it from voltage to current. This current will control the levels of the memristors M1 and M2. The resistance R3 is used to tune the amount of the current input to each memristor in order to have them switching their states as simultaneously as possible. Ideally the value of R3 is set so that it is in the middle giving same portions of current to M1 and M2. However, due to the forward voltage of the diode in the memristor emulator itself, a small tuning shift might be required to have a simultaneous shift of the memristors levels. Figure 56 shows two outputs generated from the circuit with phase difference of 180 degrees at different Vsig levels.




(a) (b)

Figure 56: (a) The input Vc and output voltage Vo when Vsig = 0v (b) The input Vc and output voltage Vo when when Vsig = 5v

Analyzing the operation of the circuit mathematically assuming a small signal Vc applied and using superposition.

$$Vo = \frac{V_c}{R_3}\,(M1 - M2) \tag{4.6}$$

In equation (4.6), If Vsig = 0v, M1 = $R_{LOW}$ and M2 = $R_{HIGH}$. Resulting in

$$Vo = \frac{V_c}{R_3}\,(R_{ON} - R_{OFF}) \approx -\frac{V_c}{R_3}\,R_{OFF} \tag{4.7}$$

In equation (4.6), If Vsig = 5v, M1 = $R_{HIGH}$ and M2 = $R_{LOW}$. Resulting in

$$Vo = \frac{V_c}{R_3}\,(R_{OFF} - R_{ON}) \approx \frac{V_c}{R_3}\,R_{OFF} \tag{4.8}$$

Equations (4.7) and (4.8) show the behavior of the circuit and how the phase will change from 0 to 180 degrees. Figure 57 shows the output of terminal w of CFOA2 and CFOA3 when Vsig = 5v and the output of terminal w of CFOA2 and CFOA3 when Vsig = 0v.

The circuit emulator used is the one shown in Figure 22 with capacitors Ci and Cd of 100nF, a shunt resistor was placed across Ci with value of 47kΩ to have a non-ideal integrator in order to avoid saturation on the capacitor Ci, Rd is a variable resistor with a maximum of 50kΩ, two resistances, 9.1kΩ and 3kΩ, with a diode in series with the 3kΩ resistance and variable resistance set to 3kΩ is the one connected to terminal Z and Y of the non-linear circuit of the emulator.

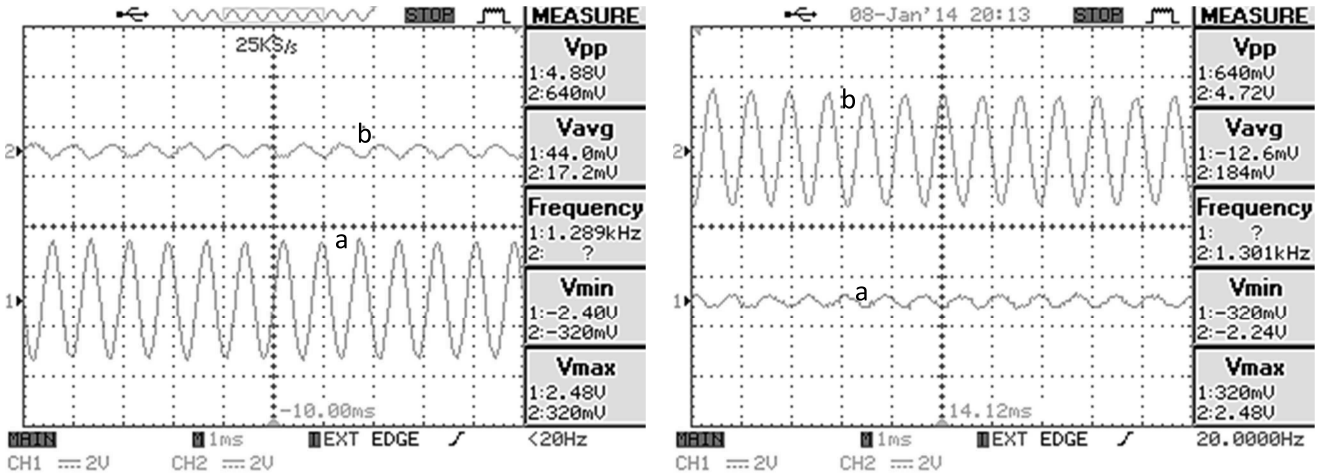



Figure 57: (a) The output voltage vs. time of terminal w of CFOA2 (a) and CFOA3 (b) when Vsig = 5v and (b) the output voltage vs. time of terminal w of CFOA2 (a) and CFOA3 (b) when Vsig = 0v

The circuit in Figure 55 operates fine when inspected one level at a time. However, one must see the transient behavior and the behavior of the circuit when applying a continuous stream through Vsig. Figure 58 shows the response of the circuit when applying a square signal in Vsig. One can notice that the phase changes occur after a small delay. This delay is caused by the discharge time in integrating capacitor in the circuit emulator itself. This puts a limitation on the frequency of the applied signal.

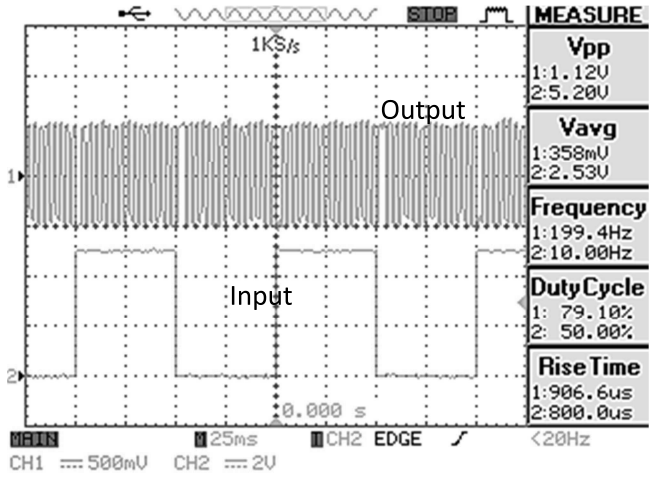



Figure 58: The output BPSK waveform and an input stream vs. time.

A simple system was implemented to modulate a signal and then demodulate it to have further insight into the performance. The system shown in Figure 59 uses the circuit in Figure 55 to modulate a signal and then retrieve it at the output Vm. The circuits used for each block are shown in Figure 60. A voltage limiter was used to have unified voltage output for both the phases from the BPSK circuit. A summing circuit will add the output from the voltage limiter circuit with the original message signal. This will make the opposite phases have less amplitude than the output with similar phase as the input carrier signal. An envelope follower is used to convert the amplitude shift keying output of the summing circuit to a square signal. A voltage comparator is used to condition the output

signal from the envelope detector so that it is a perfect square signal with amplitude from zero to five volts. The outputs from each block are shown in Figure 61. The time delay can be noticed clearly in Figure 61 (d).

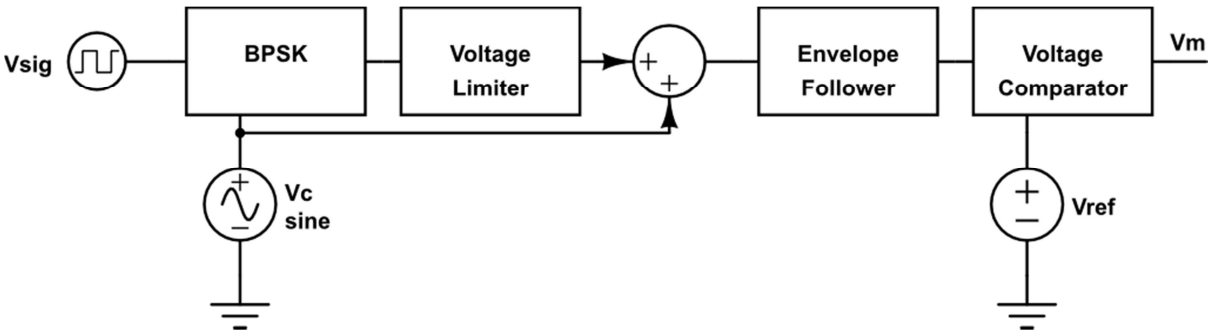



Figure 59: Overall diagram of a BPSK modulation and demodulation system

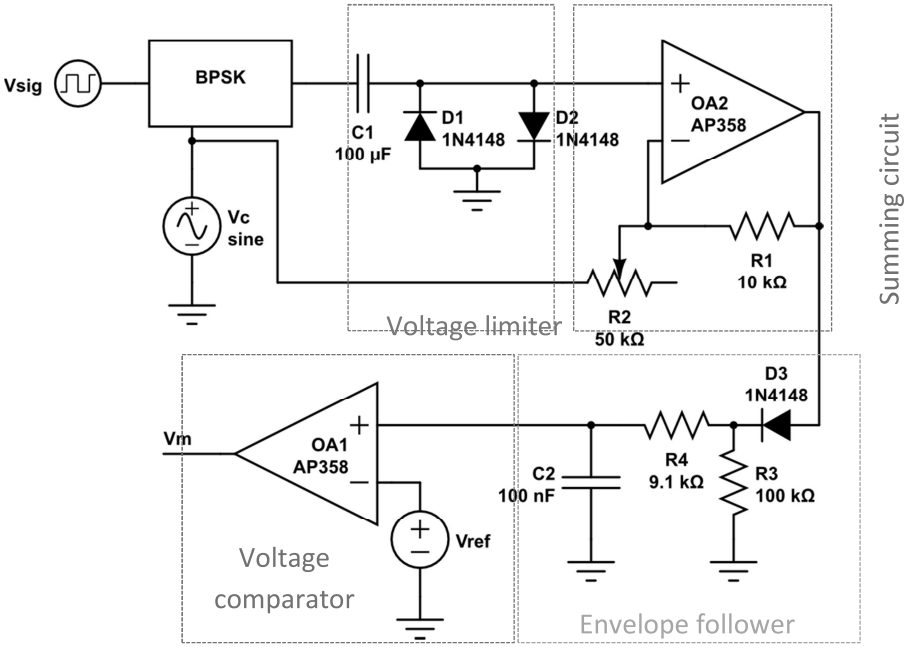



Figure 60: The circuit diagram of the BPSK modulation/demodulation system

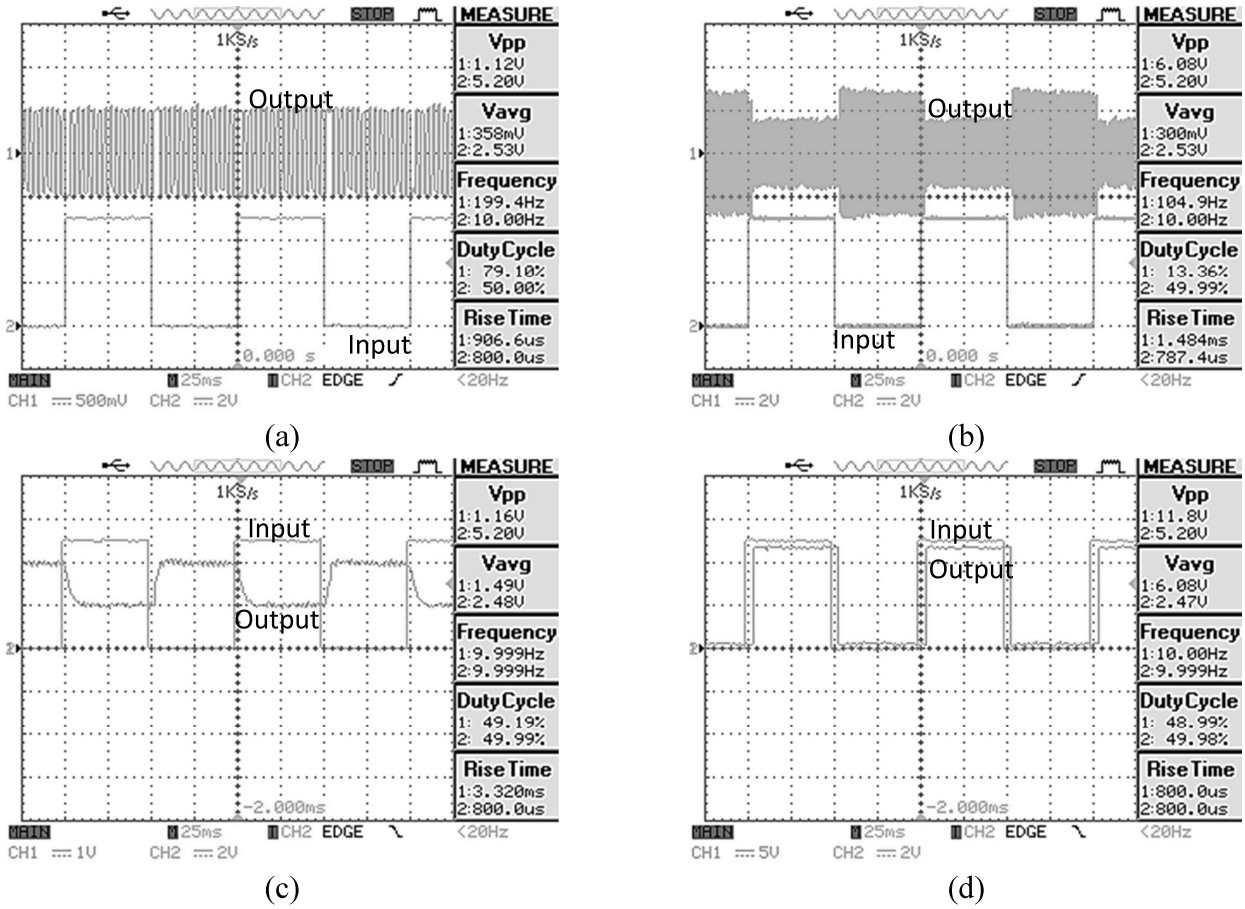



Figure 61: (a) The output and the input signal after the voltage limiter block. (b) The output and the input signal after the summing circuit block. (c) The output and the input signal after the envelope follower block. (d) The output and the input signal after the comparator block.

## 3.3. Memristor Based Sinusoidal Oscillator

The memristor can be used as a resistor in sinusoidal oscillators taking into advantage its small size in integrated circuitry. However, the memristance will oscillate as the current passing through the memristor oscillates. This change in the memristance value must be taken into consideration when designing a memristor based oscillator. If the variation in the memristance was high, the output will be distorted sinusoidal because of the non-linearity of the memristor. However, as the frequency of oscillation is increased, the voltage level after the integrator, referring to Figure 22, will be small.

Thus, the dynamic range on the diode circuit will be small enough to operate in a linear region. The emulator used is shown in Figure 22 with a shunt resistor on the integrating capacitor to avoid saturation in the integrating circuit.

Here, a Wien-bridge oscillator is built and tested by replacing one of its resistors by a memristor as shown in Figure 62. The oscillator is governed by the characteristics equation (4.9). Using Barkhausin criterion, the oscillation frequency is given in equation (4.10) and the condition of oscillation is given in equation (4.11).

$$s^2 C_1 C_2 R_1 M + s\left(C_1 R_1 + C_2 M - C_1 M \frac{R_3}{R_4}\right) + 1 = 0 \tag{4.9}$$

$$w = \frac{1}{\sqrt{C_1 C_2 R_1 M}} \tag{4.10}$$

$$C_1 M \frac{R_3}{R_4} \geq C_1 R_1 + C_2 M \tag{4.11}$$

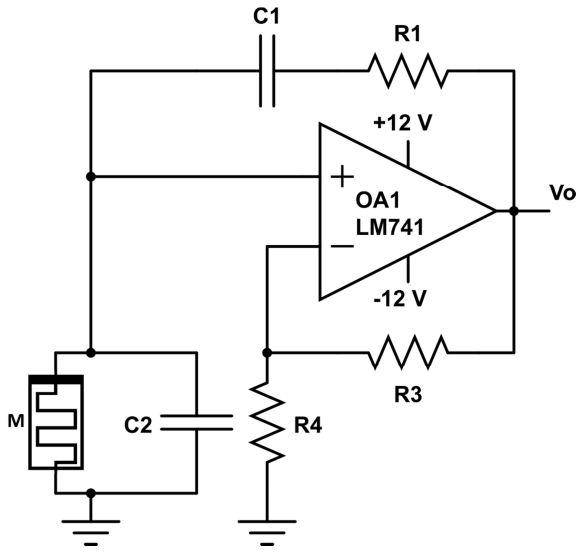



Figure 62: Wien Bridge oscillator using memristor – replacing R2

The circuit in Figure 62 was implemented using $R_1 = 33k\Omega$ and $C_1 = C_2 = 6.8nF$. $R_3$ $and$ $R_4$ were tuned to have a sinusoidal oscillation using a variable resistor with $R_3 + R_4 = 50k\Omega$. The resulted waveform is shown in Figure 63. The memristance

at the frequency of oscillation, 3.558 kHz, can be found to be $M = 1.311k\Omega$. This value is the average memristance at which this oscillation is taking place.

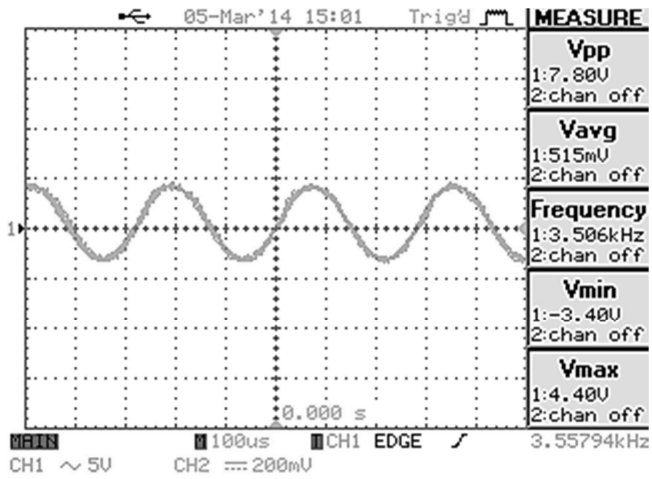



Figure 63: Result waveform from the implementation of Figure 62

Figure 64 shows another version to Figure 62 by replacing $R_4$ with the memristor. The circuit was implemented using $R_1 = R_2 = 6.8k\Omega$ and $C_1 = C_2 = 6.8nF$. $R_3$ was tuned to have a sinusoidal oscillation using a variable resistor at $R_3 = 6.67k\Omega$. The resulted waveform is shown in Figure 65. Using the characteristics equation (4.12) and applying Barkhausin criterion, the oscillation frequency is given in equation (4.13) and the condition of oscillation is given in equation (4.14). The frequency of oscillation obtained experimentally as 3.69 kHz and the frequency calculated is equal 3.44 kHz using equation (4.13). Using equation (4.14), M must be less than or equal to 2.2 kΩ which is reasonable.

$$s^2R^2C^2 + sCR\left(2 - \frac{R_3}{M}\right) + 1 = 0,$$
$$where\ R_1 = R_2 = R\ and\ C_1 = C_2 = C \tag{4.12}$$

$$w = \frac{1}{RC} \tag{4.13}$$

$$\frac{R_3}{M} \geq 2 \tag{4.14}$$

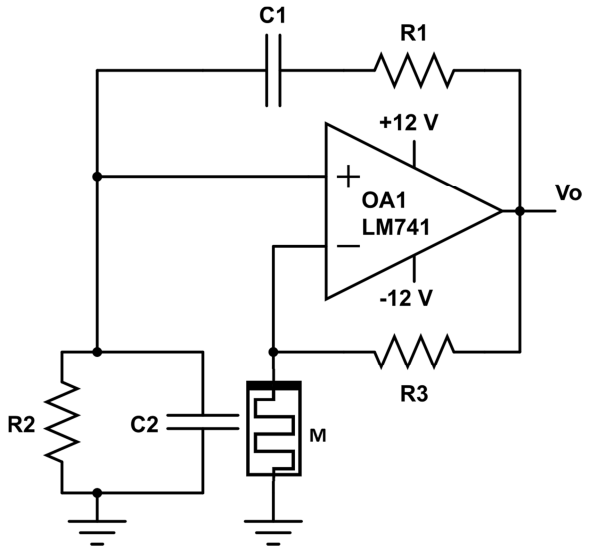



Figure 64: Wien Bridge oscillator using memristor – replacing R4

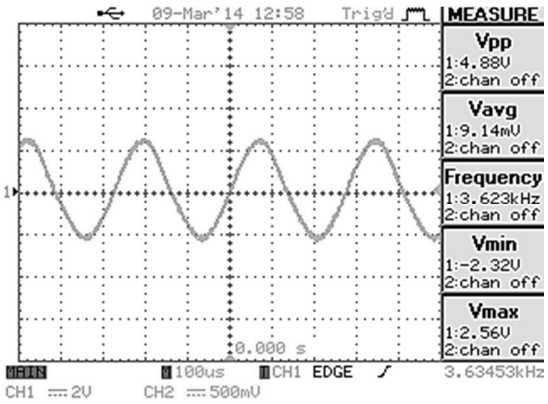



Figure 65: Result waveform from the implementation of Figure 64

## 3.4. Memristor Based Chaotic Oscillators

The memristor is used as the non-linear component in the chaotic oscillator shown in Figure 66. The circuit is based on the Wien-bridge oscillator used in Figure 62 but the value of the gain was tuned by changing the value of $R_3$ so that the memristance variation is significant to have non-linear behavior. This is because the voltage after the integrator,

referring to Figure 22, is high enough to have the diode oscillates between its forward and cutoff region.

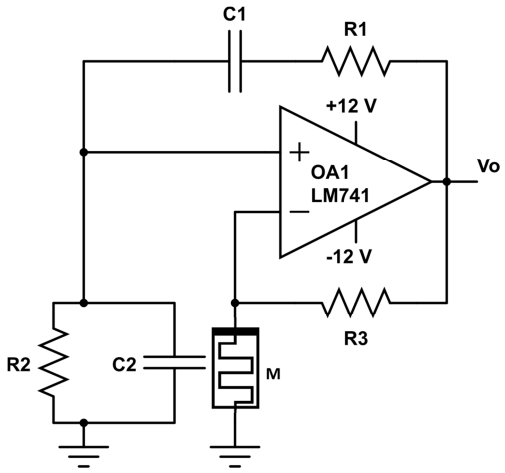



Figure 66: Chaotic oscillator circuit using memristor circuit emulator

The circuit of Figure 66 was implemented using $R_1 = 6.8k\Omega$ and $C_1 = C_2 = 6.8nF$. $R_3$ were tuned to have a chaotic oscillation using a variable resistor with $R_{3max} = 50k\Omega$. The resulted waveforms are shown in Figure 67 where the two voltage waveforms were probed from the two terminals of the capacitor $C_1$.

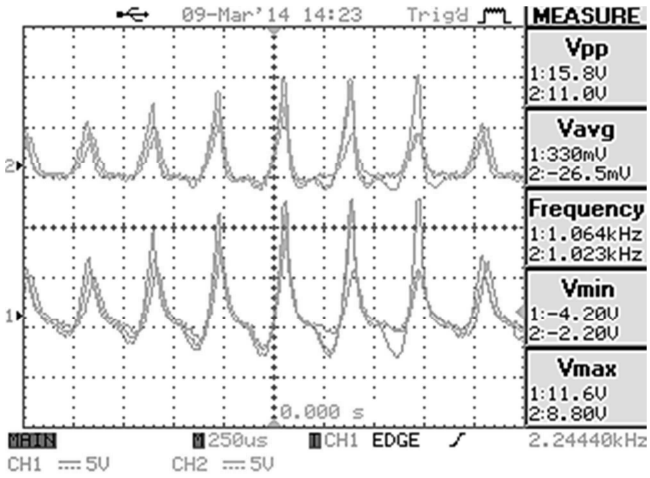



Figure 67: The two voltage waveforms were probed from the two terminals of the capacitor$C_1$.

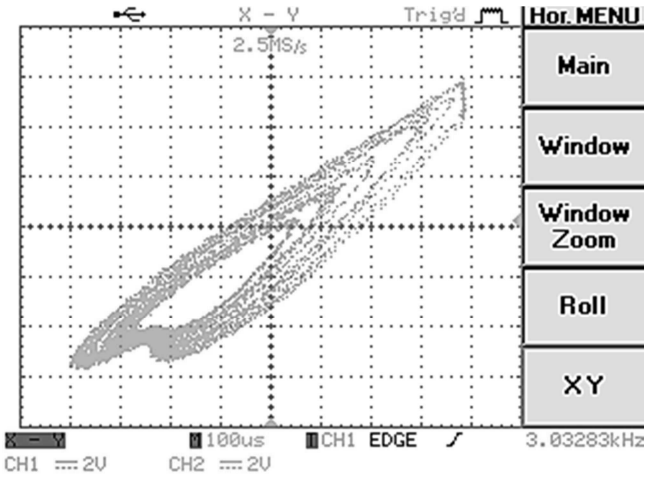



Figure 68: The X-Y representation of the voltages shown in Figure 67

By increasing the gain further, one can obtain the X-Y representation shown in Figure 69. The figure indicates that the oscillation voltage is increasing gradually until it reaches the point where the diode, in the emulator of Figure 22, reaches a level that results in violating the condition of oscillation. When the condition of oscillation is not satisfied, the voltage will saturate. This will revert the memristance value to a value that satisfies the condition of oscillation resulting in two oscillations running together producing this result.

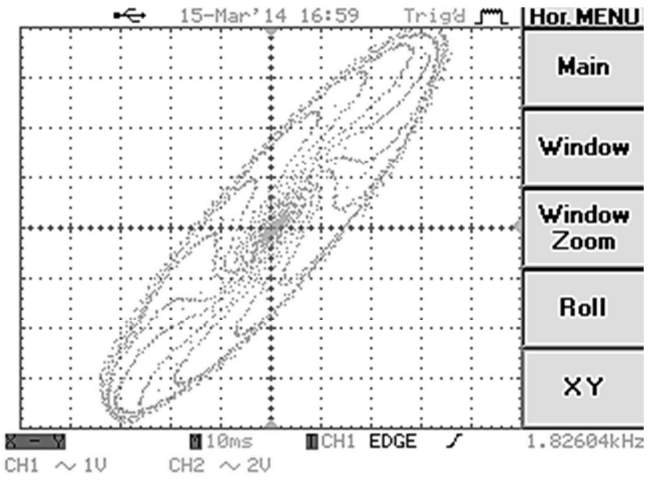



Figure 69: The X-Y representation of the voltages shown in Figure 69 with higher gain value.

# Chapter 4

# Conclusion

Different memristor emulators have been studied and some have been proposed. The proposed emulators offer different advantages and properties to suit different applications and circuit conditions. These emulator types include voltage or current driven emulator, floating or grounded emulator, discrete or continuous memristance level emulator, multi-state levels emulator, incremental or decremental emulator and finally a negative memristor emulator. Some memristor-based applications have been implemented and tested. Applications in digital modulation such as amplitude shift keying, frequency shift keying and binary phase shift keying. Other applications include sinusoidal oscillator, multivibrating oscillator and chaotic oscillator.

The memristor holds promise to replace the use of resistors in circuits thus reducing the size on chips. However, the variation in its value must be taken into considerations not to affect the application. The variation itself is useful and can be used to replace capacitors. This has been shown in the multivibrating oscillator application. The use of such advantage can be very beneficial when a very low frequency is needed such as in medical applications to avoid the use of large values of capacitors as well as resistors. Not to mention the different possibilities of using the memristor in very high frequency applications as well. The non-linearity of the memristor is also useful in chaotic oscillators and can give more variations to what is already there in the literature.

In summary, the memristor offers new possibilities to improve the current circuitries in the size on chips and variety of applications.

# References


1. D.B. Strukov, G.S. snider, D.R. Stuwart, R.S. Williams, "The missing memristor found," Nature 453, pp. 80-83, 2008.

2. Williams, R., "How We Found The Missing Memristor," *IEEE Spectrum,* vol.45, no.12, pp.28,35, Dec. 2008.

3. Z.Biolek, D.Boilek, V.Biolkova, "SPICE model of Memristor with nonlinear dopant drift," Radioengineering, vol.18, pp.210- 214, 2009

4. Chua, L.O.; Sung Mo Kang, "Memristive devices and systems," *Proceedings of the IEEE* , vol.64, no.2, pp.209,223, Feb. 1976

5. Chua, L.O. "Memristor-the missing circuit element," IEEE Transactions on Circuit Theory, vol. 18, no. 5, pp. 507–519, 1971.

6. Kvatinsky, S.; Friedman, E.G.; Kolodny, A.; Weiser, U.C., "TEAM: ThrEshold Adaptive Memristor Model," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol.60, no.1, pp.211,221, Jan. 2013

7. Biolek, D.; Bajer, J.; Biolkova, V.; Kolka, Z., "Mutators for transforming nonlinear resistor into memristor," *Circuit Theory and Design (ECCTD), 2011 20th European Conference on* , vol., no., pp.488,491, 29-31 Aug. 2011

8. Fitch, A.L.; Iu, H.H.-C.; Wang, X. Y.; Sreeram, V.; Qi, W. G., "Realization of an analog model of memristor based on light dependent resistor," *IEEE International Symposium on Circuits and Systems (ISCAS), 2012* , vol., no., pp.1139,1142, 20-23 May 2012

9. Yu, D.S.; Liang, Y.; Chen, H.; Iu, H.H.C., "Design of a Practical Memcapacitor Emulator Without Grounded Restriction," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol.60, no.4, pp.207,211, April 2013

10. E. Minayi and I.C. Goknar, "Realization of a 4-port generalized mutator and its application to memstor simulations," Proceedings of the 8th International Conference on Electrical and Electronics Engineering, 2013, (5 pages)

11. M.P. Sah, C. Yang, H. Kim and L. Chua, "A voltage mode memristor bridge synaptic circuit with memristor emulators," Sensors, Vol. 12,2012, pp. 3587-3604

12. B. Muthuswamy, "Implementing memristor based chaotic circuits, International Journal of Bifurcation and Chaos," Vol. 20, 2010, pp. 1335-1350

13. J. Valsa, D. Biolek and Z. Biolek, "An analogue model for the memristor," International Journal of Numerical Modeling: Electronic Networks, Devices and Fields, Vol. 24, 2011, pp. 400-408

14. YV. Pershin and M.D. Ventra, “Practical approach to programmable analog circuits with memristors,” IEEE Transactions on Circuits and Systems -I: Regular Papers, Vol. 57,2010, pp. 1857-1864

15. Z. Kolka, D. Biolek and V. Biolkova, “Hybrid modelling and emulation of mem-systems,” International Journal of Numerical Modeling: Electronic Networks, Devices and Fields, Vol. 25, 2012, pp. 216-225

16. Biolek, D. (2014), Memristor Emulators, in Andrew Adamatzky & Leon Chua, ed., 'Memristor Networks', Springer International Publishing, pp. 487-503.

17. Analog Devices: 4-quadrant analog multiplier AD633JN, Data Sheet. http://www.analog.com

18. M.Affan Zidan, Hesham Omran, A. G. Radwan, K. N. Salama, “Memristor-Based Reactance-Less Oscillator,” Electronics Letters, 47, 22, 1220–1221, 2011.

19. Fouda, M. E. and Radwan, A.G., “Memristor-based voltage-controlled relaxation oscillators”, International Journal of Circuit Theory and Applications, 2013

20. Tsung-Wen Lee; Nickel, J.H., "Memristor Resistance Modulation for Analog Applications," *IEEE Electron Device Letters*, vol.33, no.10, pp.1456,1458, Oct. 2012

21. Goknar, I.C.; Oncul, F.; Minayi, E., "New Memristor Applications: AM, ASK, FSK, and BPSK Modulators," *IEEE Antennas and Propagation Magazine*, vol.55, no.2, pp.304,313, April 2013

22. Werner, D.H.; Gregory, M.D., "The memristor in reconfigurable radio frequency devices," *IEEE Antennas and Propagation Society International Symposium (APSURSI), 2012*, vol., no., pp.1,2, 8-14 July 2012

23. MAKOTO ITOH, LEON O. CHUA, ”Memristor Oscillators”, *International Journal of Bifurcation and Chaos, vol* 18, no.11,pp.3183-3206 (2008).

24. A. Talukdar, A. G. Radwan, K. N. Salama, “Generalized model for memristor-based Wien family oscillators”, Microelectronics Journal vol. 42, pp. 1032–1038, 2011.

25. Laiho, M.; Lehtonen, E., "Arithmetic operations within memristor-based analog memory," *Cellular Nanoscale Networks and Their Applications (CNNA), 2010 12th International Workshop on* , vol., no., pp.1,4, 3-5 Feb. 2010

26. Berdan, R.; Prodromakis, T.; Toumazou, C., "High precision analogue memristor state tuning," *Electronics Letters* , vol.48, no.18, pp.1105,1107, August 30 2012

27. Sangho Shin; Kim, Kyungmin; Kang, S.-M.S., "Memristor Applications for Programmable Analog ICs," *IEEE Transactions on Nanotechnology*, vol.10, no.2, pp.266,274, March 2011

# Vitae

- Zainulabideen Jamal Khalifa
- Born in Jeddah, Saudi Arabia, in 1987.
- Received the B.Sc. degree in Electrical Engineering in 2009 from King Fahd University of Petroleum and Minerals (KFUPM), Dhahran, Saudi Arabia.
- Completed Master's degree requirements in Electrical Engineering at King Fahd University of Petroleum and Minerals (KFUPM), Dhahran, Saudi Arabia in 2014.
- Email: zainkhalifa@gmail.com